SPECTRUM DIGITAL INCORPORATED

TMS320VC5509 Evaluation Module

Technical Reference

2001 ***DSP Development Systems***

TMS320VC5509
Evaluation Module
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5509 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320VC5509 Digital Signal Processor.

The TMS320VC5509 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5509 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5509 will sometimes be referred to as the C55XX.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX Users Guide
Texas Instruments TMS320VC55XX Fixed Point Assembly Language Users Guide
Texas Instruments TMS320VC55XX Fixed Point C Language Users Guide
Texas Instruments TMS320VC55XX Code Composer Studio Users Guide

Table 1: Manual History

Revision	History
A	- Initial release
B	- Text correction
C	- Text correction

Chapter 1

Introduction to the TMS320VC5509 Evaluation Module

Chapter One provides a description of the TMS320VC5509 Evaluation Module along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320VC5509 EVM

The TMS320VC5509 evaluation module(EVM) is a stand-alone card. It allows evaluators to examine certain characteristics of the C5509 digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320VC5509 family of processors.

The EVM allows full speed verification of VC5509 code. With 128K words of on-chip RAM memory, 4 megawords of onboard DRAM memory, Flash ROM, Universal Serial Bus (USB), and a TLV320AIC23 stereo codec, the board can solve a variety of problems as shipped. Four expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, Code Composer Studio is available.

1.1 Key Features of the TMS320VC5509 EVM

The VC5509 EVM has the following features:

- VC5509 operating at 120 MHz.
- TLV320AIC23 Stereo Code with line and headphone interfaces
- Universal Serial Bus (USB) interface
- 128 x 64 Liquid Crystal Display (LCD)/ 9 key keypad with Jog Wheel and potentiometers
- 4 Expansion Connectors (data, I/O, control, and Host Port Interface)
- Media Card and Memory Stick Interfaces
- 4 Meg x 16 DRAM
- 1 Meg x 16 Flash Memory
- 8 Kilobyte SPI Flash Memory (not supported on Revision A of EVM)
- Embedded 1149.1 JTAG Emulation
- +5 volt operation

1.2 Functional Overview of the TMS320VC5509 EVM

Figure 1-1 shows a block diagram of the basic configuration for the VC5509 EVM. The major interfaces of the EVM include the target DRAM and ROM interface, USB, memory stick, MMC, embedded JTAG interface, codec, and expansion interface.

The VC5509 interfaces to 4 meg words of onboard DRAM and 1 megaword of Flash. An external interface supports expansion connectors for developers. A Flash Boot ROM is mapped into the external memory space. Stereo jacks provide input and outputs to and from the codec.

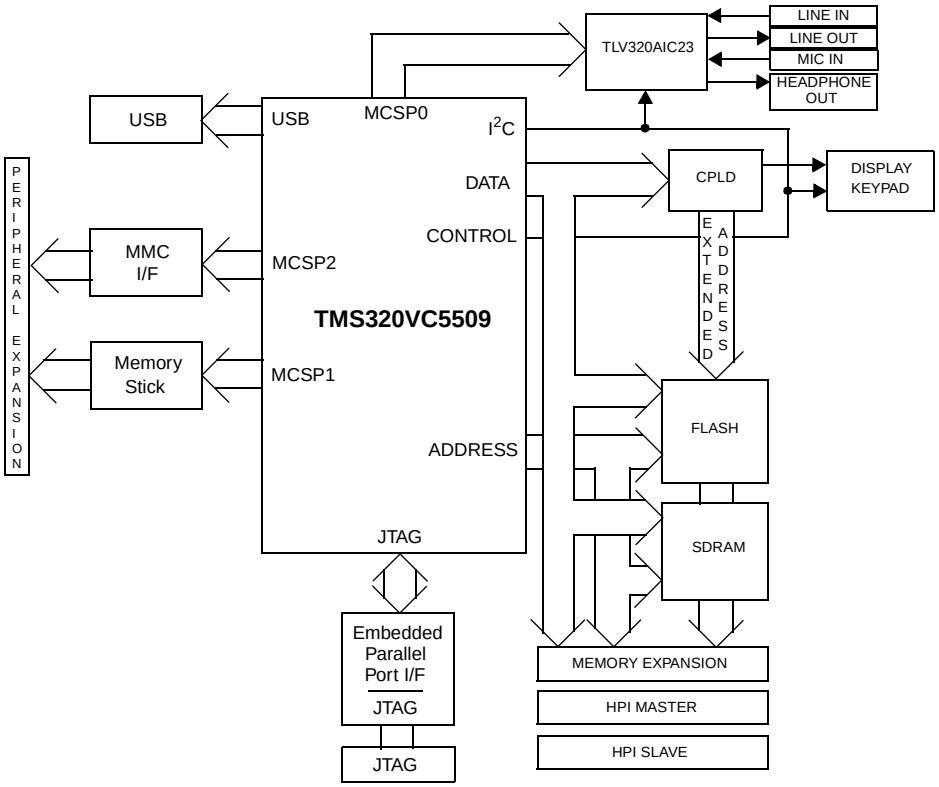

Figure 1-1, BLOCK DIAGRAM TMS320VC5509 EVM

1.3 Display/Keypad Overview

The universal display/keypad module interfaces to the EVM via a 16 pin 2mm. ribbon cable.

The display features a 128 x 64 LCD, 2 I^2C A/D converters, 2 potentiometers, 9 user keys, and a jog wheel.

Figure 1-2 below shows a block diagram of the display/keypad module.

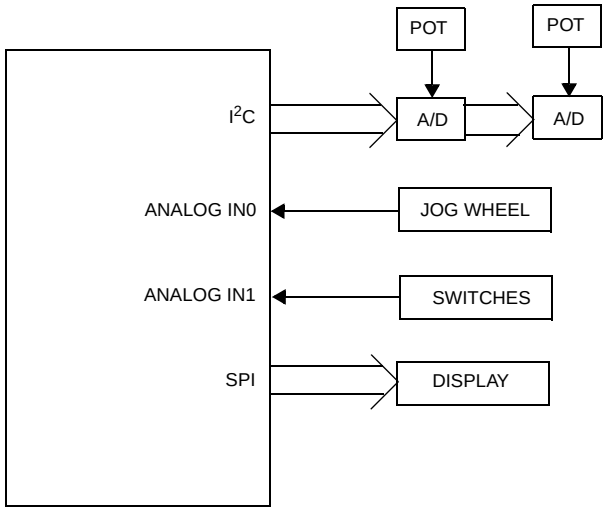

Figure 1-2, BLOCK DIAGRAM OF DISPLAY/KEYPAD

Chapter 2

Operation of the TMS320VC5509 Evaluation Module

This chapter describes the operation of the TMS320VC5509 Evaluation Module, the key interfaces and an outline of the circuit board.

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2.0 The TMS320VC5509 EVM Operation

This chapter describes the VC5509 evaluation module, key components, and how they operate. It also provides information on the EVM's various interfaces.The VC5509 EVM consists of five major blocks of logic.

- C5509 external memory
- Analog Interface
- On board Serial I/O interface
- Expansion interface
- JTAG Interface

2.1 The TMS320VC5509 EVM Board

The VC5509 EVM is a 7.0 x 3.45 inch multi-layer board which is powered by an external +5 volt only power supply. Figure 2-1 shows the top and bottom layout of the VC5509 EVM.

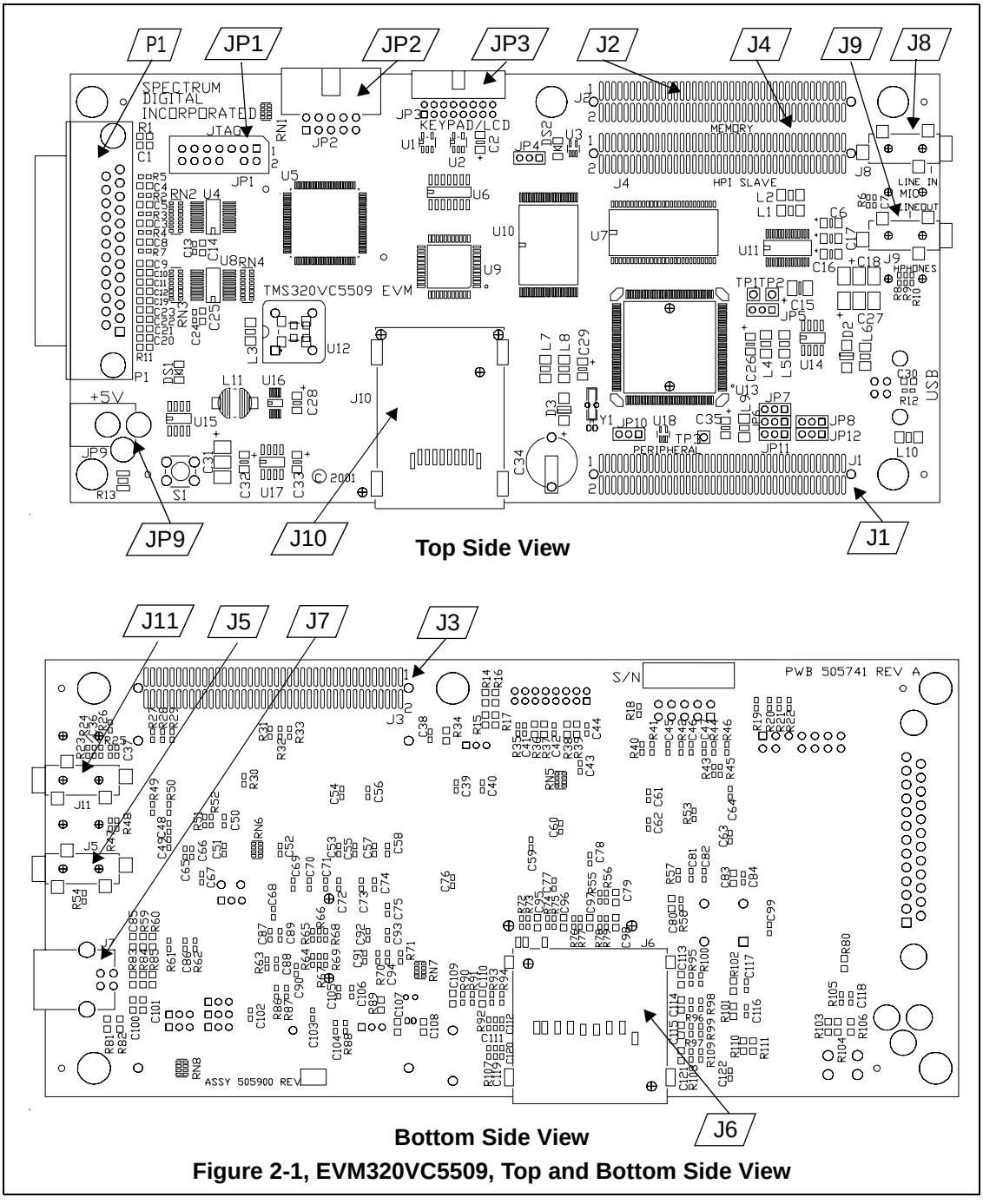


Figure 2-1, EVM320VC5509, Top and Bottom Side View

2.1.1 Power Connector

The VC5509 is powered by a +5 volt only power supply which is available with the module. The board requires 1 amp. The power is supplied via 2 millimeter jack JP9. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board also has a +3.3 and +1.5 volt regulator to provide power to the lower voltage components.

2.2 TMS320VC5509 Memory Interface

The next several sections describe the various memory interface present on the TMS320VC5509 EVM.

The memory map of the VC5509 EVM is shown below.

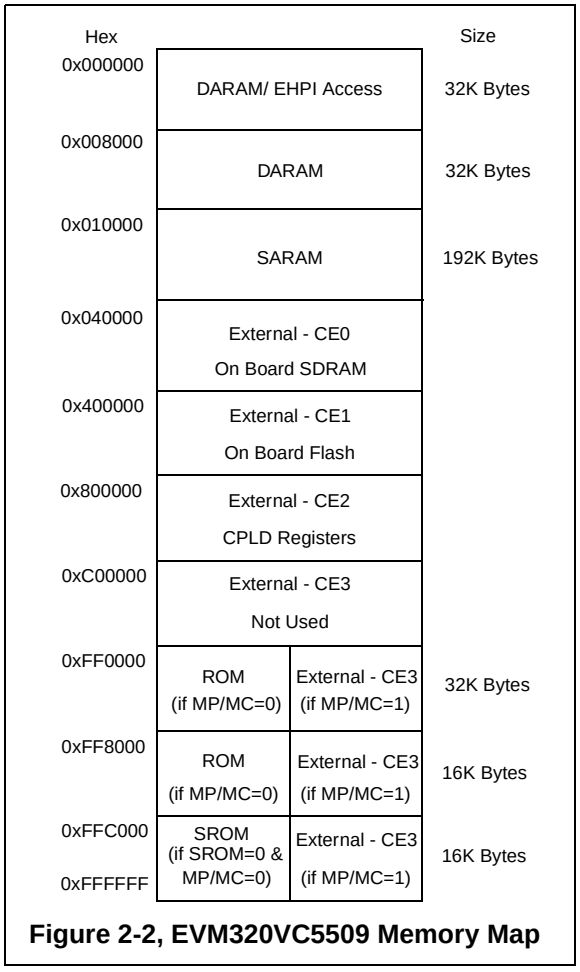


Figure 2-2, EVM320VC5509 Memory Map

2.2.1 SDRAM Interface

The VC5509 directly interfaces to SDRAM. On the EVM the SDRAM is mapped into the VC5509's CE0 space allowing 4 megabytes of on board DRAM. The DRAM is controlled by on chip control registers. For proper configuration of these registers refer to the VC5509 demonstration code included with the EVM.

2.2.2 Interface CPLD

The VC5509 uses a CPLD to interface to the Flash ROM, host port, and SPI for the display. The CPLD is mapped into the CEn address space and contains on 8-bit extended address register for the Flash Memory, an 8-bit shift register for the SPI control to the display, and an Address Decoder for the Host Port Interface.

The addresses are defined below for 16 bit access (i.e. (volatile unsigned short *));

Table 1: CPLD Memory Mapping

Function	Address
Extended Address Latch	0x401000
Display Address 0	0x401800
Display Address 2	0x401808
Host Port Chip Select	????

2.2.3 Flash ROM

The Flash ROM typically resides in the CE1 space. Since the VC5509 144 pin PGE package only supplies 12 address lines directly the upper 8 address bits for the Flash ROM are supplied by the CPLD, U9. At reset these extended address lines are set to 0. The extended address latch format is shown below.

Table 2: Extended Address Latch 0x401000

D7	D6	D5	D4	D3	D2	D1	D0
Ext Add 7	Ext Add 6	Ext Add 5	Ext Add 4	Ext Add 3	Ext Add 2	Ext Add 1	Ext Add 0

2.2.4 LCD Interface

The Liquid Crystal Display (LCD) is a write only interface. It is interfaced via an 8-bit shift register.

Two locations are used to interface the LCD address bit to be directly programmed. Writing to these locations starts the output to be serialized in an 8 bit sequence to the display. The shift clock frequency is 3 megahertz.

The address location 0x401800 LCD A0 should = 0. Address location 0x401800 can be addressed when LCD A0 = 1.

The table below shows the relationship of the DSP data bits to the LCD data bits.

Table 3: Extended Address Latch 0x401000

D7	D6	D5	D4	D3	D2	D1	D0
LCD D7	LCD D6	LCD D5	LCD D4	LCD D3	LCD D2	LCD D1	LCD D0

The figure below shows the LCD data transfer timing.

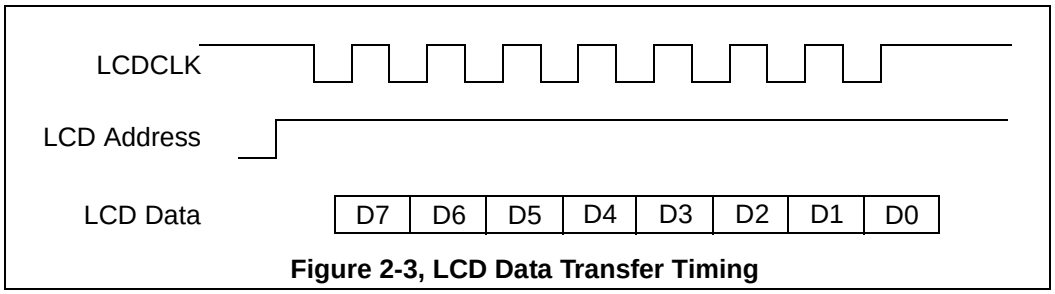


Figure 2-3, LCD Data Transfer Timing

The status of the shift register is put out on GPIO4. When high, the LCD shift register is busy. When GPIO4 is low the shift register is ready.

2.3 Oscillator Selection

The TMS320VC5509 EVM is equipped with a 24 megahertz oscillator. This oscillator runs the on board parallel port JTAG controller. This clock is divided by resulting in a 12 megahertz clock which is used to drive the VC5509. This frequency is used to be compatible with USB timing requirements.

2.4 EVM320VC5509 Connectors

The TMS320VC5509 EVM has sixteen (16) connectors which provide the user access to the various on the EVM. The position of each connector is identified in Figure 2-1.These connectors, their size, their function, and the side of the printed circuit board they are mounted on are shown in the table below.

Table 4: EVM320VC5509 Connectors

Connector	# Pins	Function	Side of Board
J1	80	Peripheral	Top
J2	80	Memory	Top
J3	80	HPI Master	Bottom
J4	80	HPI Slave	Top
J5	2	Microphone	Bottom
J6	2	MMC Card	Bottom
J7	5	USB	Bottom
J8	2	Line In	Top
J9	2	Line Out	Top
J10	10	Memory Stick	Top
J11	2	Headphones	Bottom
P1	25	Parallel Port/JTAG	Top
JP1	14	External JTAG	Top
JP2	10	CPLD Programming	Top
JP3	18	Display/Keypad	Top
JP9	2	+5 Volt	Top

Note: The HPI Master, J3 is provided to allow 2 VC5509 EVMs to be connected together from master to slave.

2.4.1 J1, Peripheral Expansion Connector for VC5509

Table 5: J1, Peripheral Expansion Connector

Pin #	Signal Name	Pin #	Signal Name
1	RESERVED	2	RESERVED
3	GND	4	GND
5	+5 Volts	6	+5 Volts
7	GND	8	GND
9	+5 Volts	10	+5 Volts
11	HD1	12	RESERVED
13	UART_TX	14	RESERVED
15	HD0	16	HD5
17	RESERVED	18	HD4
19	+3.3 Volts	20	+3.3 Volts
21	BCLKX1	22	RESERVED
23	BFSX1	24	BDX1
25	GND	26	GND
27	BCLKR1	28	RESERVED
29	BFSR1	30	BDR1
31	GND	32	GND
33	BCLKX2	34	RESERVED
35	BFSX2	36	BDX2
37	GND	38	GND
39	BCLKR2	40	RESERVED
41	BFSR2	42	BDR2
43	GND	44	GND
45	TOUT	46	RESERVED
47	RESERVED	48	INT4-
49	RESERVED	50	RESERVED
51	GND	52	GND
53	INT3-	54	RESERVED
55	RESERVED	56	ANALOG0 INPUT
57	RESERVED	58	ANALOG1 INPUT
59	RESET-	60	RESERVED
61	GND	62	GND
63	GPIO3	64	GPIO1
65	GPIO4	66	GPIO2
67	INT0-	68	INT1-
69	RESERVED	70	RESERVED
71	RESERVED	72	RESERVED
73	RESERVED	74	RESERVED
75	GND	76	GND
77	GND	78	CLKOUT
79	GND	80	GND

2.4.2 J2, Memory Expansion Connector for VC5509

Table 6: J2, Memory Expansion Connector

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 volts
3	RESERVED	4	RESERVED
5	RESERVED	6	RESERVED
7	RESERVED	8	RESERVED
9	RESERVED	10	RESERVED
11	GND	12	GND
13	A13	14	A12
15	A11	16	A10
17	A9	18	A8
19	A7	20	A6
21	+5 Volts	22	+5 Volts
23	A5	24	A4
25	A3	26	A2
27	A1	28	A0
29	GND	30	GND
31	GND	32	GND
33	RESERVED	34	RESERVED
35	RESERVED	36	RESERVED
37	RESERVED	38	RESERVED
39	RESERVED	40	RESERVED
41	+3.3 Volts	42	+3.3 Volts
43	RESERVED	44	RESERVED
45	RESERVED	46	RESERVED
47	RESERVED	48	RESERVED
49	RESERVED	50	RESERVED
51	GND	52	GND
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	GND	62	GND
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	GND	72	GND
73	RE	74	WE-
75	OE	76	RDY-
77	CE1	78	CE3-
79	GND	80	GND

2.4.3 J3, HPI Master Expansion Connector for VC5509

Table 7: J3, HPI Master Expansion Connector

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 Volts
3	RESERVED	4	RESERVED
5	RESERVED	6	RESERVED
7	RESERVED	8	RESERVED
9	RESERVED	10	RESERVED
11	GND	12	GND
13	A0	14	A13
15	A12	16	A11
17	A10	18	A9
19	A8	20	A7
21	+ 5 Volts	22	+5 Volts
23	A6	24	A5
25	A4	26	A3
27	A2	28	A1
29	BE1	30	BE0n
31	GND	32	GND
33	RESERVED	34	Hostport CE-
35	RESERVED	36	RESERVED
37	RESERVED	38	RESERVED
39	RESERVED	40	RESERVED
41	RESERVED	42	RESERVED
43	RESERVED	44	RESERVED
45	RESERVED	46	RESERVED
47	RESERVED	48	WE-
49	RESERVED	50	WE
51	GND	52	GND
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	GND	62	GND
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	GND	72	GND
73	RE	74	A13
75	INT1n	76	READY
77	A3	78	A0
79	GND	80	GND

2.4.4 J4, HPI Slave Expansion Connector for VC5509

Table 8: J4, HPI Slave Expansion Connector

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 volts
3	RESERVED	4	RESERVED
5	RESERVED	6	RESERVED
7	RESERVED	8	RESERVED
9	RESERVED	10	RESERVED
11	GND	12	GND
13	A13	14	A12
15	A11	16	A10
17	A9	18	A8
19	A7	20	A6
21	+5 Volts	22	+5 Volts
23	A5	24	A4
25	A3	26	A2
27	A1	28	A0
29	BE1n	30	BE0n
31	GND	32	GND
33	GP0	34	SDCAS
35	SDRASn	36	RESERVED
37	RESERVED	38	RESERVED
39	RESERVED	40	RESERVED
41	RESERVED	42	RESERVED
43	RESERVED	44	RESERVED
45	RESERVED	46	RESERVED
47	RESERVED	48	RESERVED
49	RESERVED	50	CLKMEM
51	GND	52	GND
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	GND	62	GND
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	GND	72	GND
73	SDWEn	74	WE
75	OEn	76	Ready
77	CE3n	78	CE2n
79	GND	80	GND

2.4.5 J11, Microphone Connector

The microphone interfaces directly to the TLV320AIC23. It is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

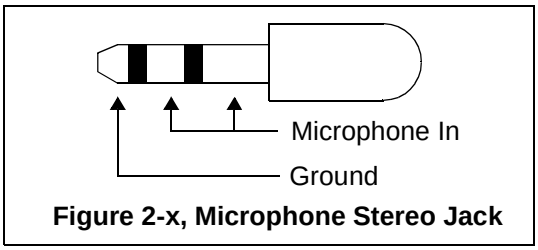


Figure 2-x, Microphone Stereo Jack

2.4.6 J6, Multi-Media Card (MMC) Connector

The VC5509 interfaces directly to a multi-media card. On the VC5509 EVM the multi-channel serial port 2 is used. The pin out for this standard 12 pin connector is shown in the table below.

Table 9: J7, MMC Connector

Pin #	MMC Signal Name	DSP Signal Name
1	DATA3	MMC2.DAT3
2	Command	MMC2.CMD
3	Vss	Ground
4	Vdd	+3.3 Volts
5	CLK	MMC2.CLK
6	Vss	Ground
7	DATA0	MMC2.DAT0
8	DATA1	MMC2.DAT1
9	DATA2	MMC2.DAT2
10	Write Protect	Not Used
11	Common	Ground
12	Insert	Not Used

2.4.7 J7, Universal Serial Bus (USB) Connector

Connector J7 provides a Universal Serial Bus (USB) Interface to the EVM320VC5509. The VC5509 has a built in USB interface peripheral.The signals on this connector are shown in the below.

Table 10: J7, USB Connector

Pin #	USB Signal Name	DSP Signal Name
1	USBVdd	Voltage Divider to GPIO7
2	D+	DP-USB
3	D-	DN-USB
4	USB Vss	Ground
5	Shield	Ground
6	Shield	Ground

Note: GPIO7 is used for USB power detection and PV DSP is used to interface to positive data signal D+;

2.4.8 J8, Audio Line In Connector

The audio line in is a stereo input. This input interfaces directly to the TLV320AIC23. The connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

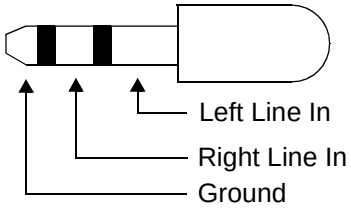


Figure 2-4, Audio Line In Stereo Jack

2.4.9 J9, Audio Line Out Connector

The audio line out is a stereo output. This output is driven directly by the TLV320AIC23. The connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

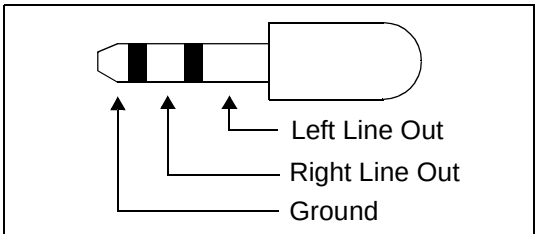


Figure 2-5, Audio Line Out Stereo Jack

2.4.10 J10, Memory Stick Connector

Connector J10 interfaces to a Memory Stick. The VC5509 drives this directly from the on chip serial port. The pin out of the memory stick is shown in the table below.

Table 11: J10, Memory Stick Connector

Pin #	Memory Stick Signal Name	DSP Signal Name
1	Vssl	Ground
2	BS	MMC1.DAT3
3	Vcc1	+3.3 Volts
4	SDIO	MMC1.DAT0
5	RESERVED	Not Used
6	XINS	MMC1.DAT2
7	RSVD	MMC1.DAT1
8	SCLK	MMC1.CLK
9	Vcc2	+3.3 Volts
10	Vss2	Ground

2.4.11 J5, Headphone Connector

Connector J5 is a headphone jack. It is driven by the TLV320AIC23 and can drive standard headphones directly. The standard 3.5 mm jack is shown in the figure below.

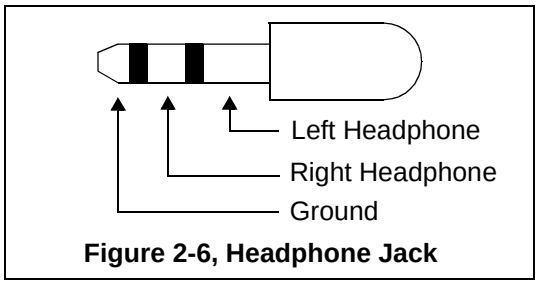


Figure 2-6, Headphone Jack

2.4.12 P1, Parallel Port/JTAG Connector

Connector P1 provides the parallel port connection back to the host PC. This is a standard 25 pin D-sub connector and interfaces to any standard bi-directional, ECP, or EPP personal computer parallel port.

2.4.13 JP1, External JTAG Connector

The TMS320VC5509 Evaluation Module is supplied with a 14 pin header interface, JP1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-6 below.

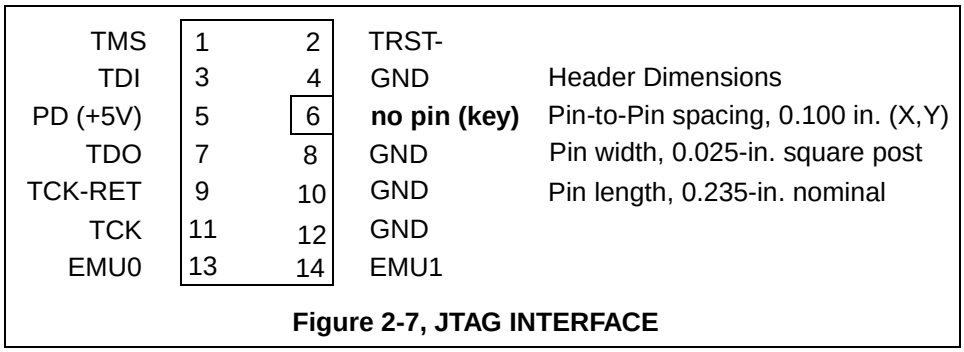


Figure 2-7, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 12: JP1, JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

2.4.14 JP2, PLD Programming Connector

This connector interfaces to the Altera CPLD, U9. It is used in the in the factory for the programming of the CPLD. This connector should not be used outside the factory.

2.4.15 JP3, Display/Keypad Interface Connector

Connector JP3 provides an interface to the universal display/keypad module. The display interfaces via an 8 bit serial interface which is designed into CPLD, U9. The switches interface via Analog Input, A1, on the VC5509. The jog wheel interfaces via Analog Input A0 on the VC5509. Two I^2C A/Ds are used to interface to the user potentiometers.

This connector has 16 pins. The signals on this connector are shown in the below.

Table 13: JP3, LCD Connector

Pin #	Signal Name	Pin #	Signal Name
1	+3.3 Volts	2	+3.3 Volts
3	Analog Input A0	4	Analog Input A1
5	LCD Serial Input	6	LCD Address 0
7	Reset	8	LCD shift Clock
9	Ground	10	Ground
11	I^2C SDA	12	Ground
13	I^2C SCLK	14	Ground
15	+3.3 Volts	16	+3.3 Volts

2.4.16 JP9, +5 Volt Connector

Power (5 volts) is brought onto the EVM VC5509 via the JP9 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2 mm. The position of the JP9 connector is shown below.

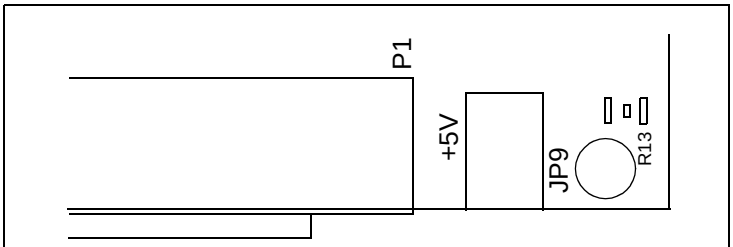


Figure 2-8, Power Connector Location

The diagram of JP9, which has the input power is shown below.

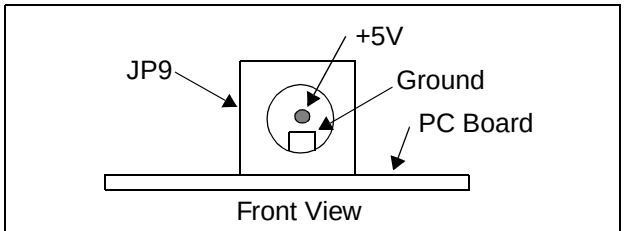


Figure 2-9, EVM VC5509 Power Connector

2.5 EVM320VC5509 Jumpers

The EVM320VC5509 has 8 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. All jumpers are accessible from the top side of the printed circuit board. The following sections describe the use of each jumper.

Table 14: EVM320VC5509 Jumpers

Jumper #	Size	Function
JP4	1 x 3	Flash ROM Chip Select
JP5	1 x 3	Codec Clock Select
JP6	1 x 3	GP3 Boot Select
JP7	1 x 3	Expansion +3.3 Volt Select
JP8	1 x 3	GP1 Boot Select
JP10	1 x 3	Real Time Clock Input
JP11	1 x 3	GP2 Boot Select
JP12	1 x 3	GP0 Boot Select

Each jumper on the TMS320VC5509 EVM is a 1x3 jumper. Each 1 x 3 jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a ‘1’ on the boards silk-screen. A top view of the 1 x 3 jumper is shown below:

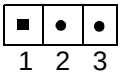


Figure 2-10, 1x3 Jumper Layout

WARNING!
Unless noted otherwise, all 1x3 jumpers must be installed in either the 1-2 or 2-3 position

2.5.1 Jumper Positions

The figure 2-11 shows the locations of the jumpers on the TMS320VC5509 EVM.

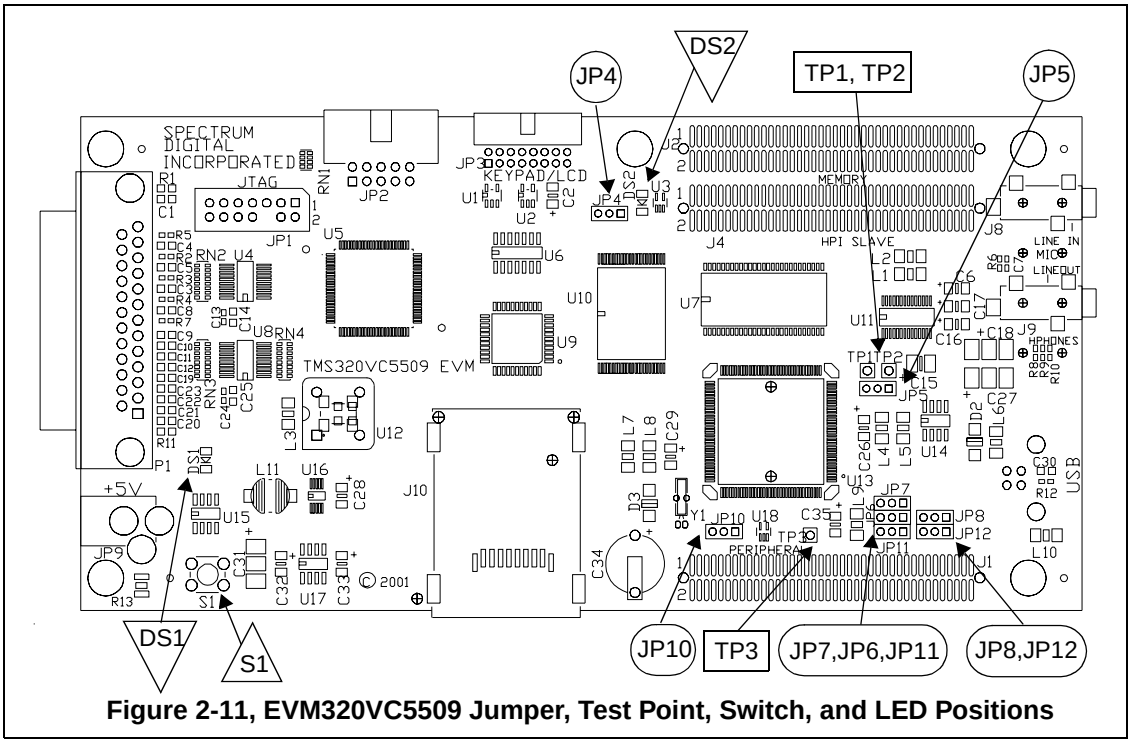


Figure 2-11, EVM320VC5509 Jumper, Test Point, Switch, and LED Positions

2.5.2 JP4, Flash ROM Chip Select

Jumper JP1 is used to select if the Flash ROM is in CE1 or CE3 space. When position 1-2 is selected the Flash ROM is in the CE1 space. The 2-3 position selects CE3 as the Flash ROM chip select. The table below shows the positions and their functions.

Table 15: JP4, Flash ROM Chip Select

Position	Function
1-2	Flash CS in CE1 space
2-3	Flash CS in CE3 space

2.5.3 JP5, Codec Clock Select

Jumper JP2 is used to determine whether the on board 12 Mhz. clock or TOUT is used to drive the codec clock. When position 1-2 is selected the on board 12 Mhz. clock drives the AIC23 input clock. The 2-3 position selects TOUT to drive the AIC23 input clock. The table below shows the positions and their functions.

Table 16: JP5, Codec Clock Select

Position	Function
1-2	12 Mhz. clock drives AIC23
2-3	TOUT drives AIC23

2.5.4 JP7, Expansion +3.3 Volt Select

Jumper JP3 is used to select if +3.3 volts is output on the expansion connector. When position 1-2 is selected the +3.3 volts is output to the expansion connectors J1, J2. If the 2-3 position is used no voltage is output on these pins. The table below shows the positions and their functions.

Table 17: JP7, Expansion +3.3 Volt Select

Position	Function
1-2	+3.3 volts on expansion connectors J1, J2
2-3	No voltage on expansion connectors

2.5.5 JP10, Real Time Clock Input

Jumper JP4 is used to select TOUT or the crystal is used as the real time clock. When position 1-2 is selected the RTCLK is driven by TOUT. When the 2-3 position is used the real time clock is driven by a 32.768K hertz crystal. The table below shows the positions and their functions.

Table 18: JP10, Real Time Clock Input

Position	Function
1-2	TOUT Selected as RTCLK source
2-3	32.768K Mhz. selected as RTCLK source

Note: Revision A of the Printed Circuit Board does **NOT** support the 1-2 option.

2.5.6 JP6, JP8, JP11, JP12 Bootload Select

Jumpers JP6, JP8, JP11, and JP12 control the bootload mode on the VC5509 EVM. When one of these jumpers is in the 1-2 position the signal is a logic 1. When the 2-3 position is selected the signal is a logic 0. The table below shows the mapping from jumper positions to the GPIO pins.

Table 19: JP6, JP8, JP11, JP12, Bootload Select

GPIO3	GPIO2	GPIO1	GPIO0	Boot Mode Process
JP6	JP11	JP8	JP12	
2-3	2-3	2-3	2-3	Reserved
2-3	2-3	2-3	1-2	16-bit asychronous memory
2-3	2-3	1-2	2-3	Serial SPI Boot (24-bit)
2-3	2-3	1-2	1-2	Serial SPI Boot (16-bit)
2-3	1-2	2-3	2-3	USB
2-3	1-2	2-3	1-2	8-bit asychronous memory
2-3	1-2	1-2	2-3	Reserved
2-3	1-2	1-2	1-2	16-bit asychronous memory
1-2	2-3	2-3	2-3	Reserved
1-2	2-3	2-3	1-2	Reserved
1-2	2-3	1-2	2-3	EHPI- multiplexed mode
1-2	2-3	1-2	1-2	EHPI- non multiplexed mode
1-2	1-2	2-3	2-3	Reserved
1-2	1-2	2-3	1-2	16-bit McBSP #0
1-2	1-2	1-2	2-3	Reserved
1-2	1-2	1-2	1-2	8-bit McBSP #0

2.6 LEDs

The EVM320VC5509 has two light emitting diodes. DS1 indicates the presence of +5 volts and is normally ‘on’ when power is applied to the board. DS2 is under software control. It is tied to the XF pin on the DSP through an inverter. These are shown in the table below.

Table 20: LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Green	+5 Volts	1
DS2	Green	XF on DSP	1

2.7 Resets

There are three resets on the TMS320VC5509 EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5509.

External sources which control the reset are push button S1, and a bit in the parallel port JTAG interface gate array

2.8 Test Points

The EVM320VC5509 has three test points. The position of each test point is shown in Figure 2-x. The signals associated with each test point are shown in the table below.

Table 21: Test Points

Test Point	Signal
TP1	AIC CLKOUT
TP2	AIC LRCLK INPUT
TP3	DSP CLKOUT

2.9 Switches

The EVM320VC5509 has one switch, S1. This is a push button reset switch which will perform a hardware reset.

Appendix A

TMS320VC5509 EVM CPLD Equations

This appendix lists the VHDL for CPLD U9, used on the TMS320VC5509 Evaluation Module (EVM).

Topic **Page**

A.1 CPLD Equations for VC5509

The following equations are used in the CPLD, U9, on the VC5509 EVM.

```
---------------------------------------------------------------------------------
-- $Archive::                                                                   $
-- $Revision::                                                                  $
-- $Date::                                                                      $
-- $Author::                                                                    $
--
--
--
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
-- Start the real code
---------------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
-- xpplus_comps.all inlcude some SD specific components that we have used
-- in several places.  This is mainly printer port and emulator logic.
-- use work.xpplus_comps.all;

entity evm5509 is
  port
  (
        iMCLK           :in std_logic;   -- Input Master clock
        iD              :in std_logic_vector( 7 downto 0 );
        iCE0n           :in std_logic;
        iA13            :in std_logic;
        iA1             :in std_logic;
        iA2             :in std_logic;
        iA3             :in std_logic;
        iWEn            :in std_logic;
        iRESETn         :in std_logic;

        oFLASH_ADD      : out std_logic_vector( 7 downto 0 );
        oLCDSI          : out std_logic;
        oLCDSCK         : out std_logic;
        oLCDA0          : out std_logic;
        oLCDBUSY        : out std_logic;
        oHOSTPORTCSn    : out std_logic;
        oFLASHCSn       : out std_logic );
end evm5509;
```

```
---------------------------------------------------------------------------------
-- Include standard librariess
---------------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
-- use work.std_arith.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

---------------------------------------------------------------------------------
-- Include fpga specifics here if required.
-- act3  is for Actel 54sx devices.  We normally use this for the hardwired
-- clock definition.
---------------------------------------------------------------------------------
-- library act3;
-- use act3.components.all;

architecture behavior_evm5509 of evm5509 is
---------------------------------------------------------------------------------
-- Add local components in here
---------------------------------------------------------------------------------
--component MyComponent
--port
--(
--);
--end component;

---------------------------------------------------------------------------------
-- Add signals
---------------------------------------------------------------------------------

--signal    SignalName          : std_logic; -- From Lpt, read/write request
  signal    ExtAddress          : std_logic_vector( 7 downto 0 );

        signal    MclkDiv         : std_logic_vector( 1 downto 0 );
        signal    LcdClkEn        : std_logic;

        signal    LcdA0           : std_logic;
        signal    LcdD            : std_logic_vector( 7 downto 0 );
        signal    LcdRequest      : std_logic;
        signal    LcdStart        : std_logic;

        signal    LcdMuxD         : std_logic;
        signal    LcdShiftCnt     : std_logic_vector( 2 downto 0 );
        signal    LcdSckOn        : std_logic;
```

```
-------------------------------------------------------------------------------
-- The implementation
-------------------------------------------------------------------------------

begin

-------------------------------------------------------------------------------
-- Actel specific definition for the hardwired clock “hclk”
-------------------------------------------------------------------------------
-- u1: HCLKBUF port map( PAD => iMasterClockIn, Y => oMasterClockIn );

-------------------------------------------------------------------------------
-- Map the other components
-------------------------------------------------------------------------------
--u2: my_component port map ( ComponentSignalName => SignalConnection, ... );


-------------------------------------------------------------------------------
-- Now define the logic
-------------------------------------------------------------------------------

--process( syncPONRSn, MCLK, ....)
--begin
--    if syncPONRSn = ‘0’ then
--    Reset the signals to default states
--  elsif MCLK’event and MCLK = ‘1’ then
--  end if;
--end process;


 -- Extended address latch.
        -- Set to 0 on reset.
        -- Write on the rising edge of iWEn
        -- A 1-000
        process( iWEn, iRESETn, iCE0n, iA13, iA3, iA2, iA1, iD )
        begin
          if iRESETn = ‘0’ then
                ExtAddress <= ( others => ‘0’ );
             elsif iWEn’event and iWEn = ‘1’ then
               if (      iCE0n = ‘0’
                  and  iA13  = ‘1’
                  and  iA3   = ‘0’
                  and  iA2   = ‘0’
                  and  iA1   = ‘0’ ) then
                  ExtAddress <= iD;
                  end if;
             end if;
        end process;
```

```
      oFLASH_ADD <= ExtAddress;

      -- Host port A 1-110
oHOSTPORTCSn <= '0' when (    iCE0n   = '0'
            and  iA13  = '1'
            and  iA3   = '1'
            and  iA2   = '1'
            and  iA1   = '0' ) else '1';

-- Flash A  0-xxx
oFLASHCSn   <= '0' when (       iCE0n   = '0'
            and  iA13    = '0' ) else '1';


      -- ##########################################################################
      -- LCD
      --

      -- Create a divide by 4 clock with a LcdClkEn.
      -- DivClk    LcdClkEn
      --   00        0
      --   01        0
      --   10        1
      --   11        0
      -- All states operate on Mclk when LcdClkEn = '1'.
      -- A 1-100
      -- A 1-101
      --
process( iRESETn, iMCLK )
      begin
        if iRESETn = '0' then
            MclkDiv  <= (others => '0' );
            LcdClkEn <= '0';
            elsif iMCLK'event and iMCLK = '1' then

              MclkDiv <= MclkDiv + 1;

              if( MclkDiv = "10" ) then
                 LcdClkEn <= '1';
              else
                 LcdClkEn <= '0';
              end if;
            end if;
      end process;
```

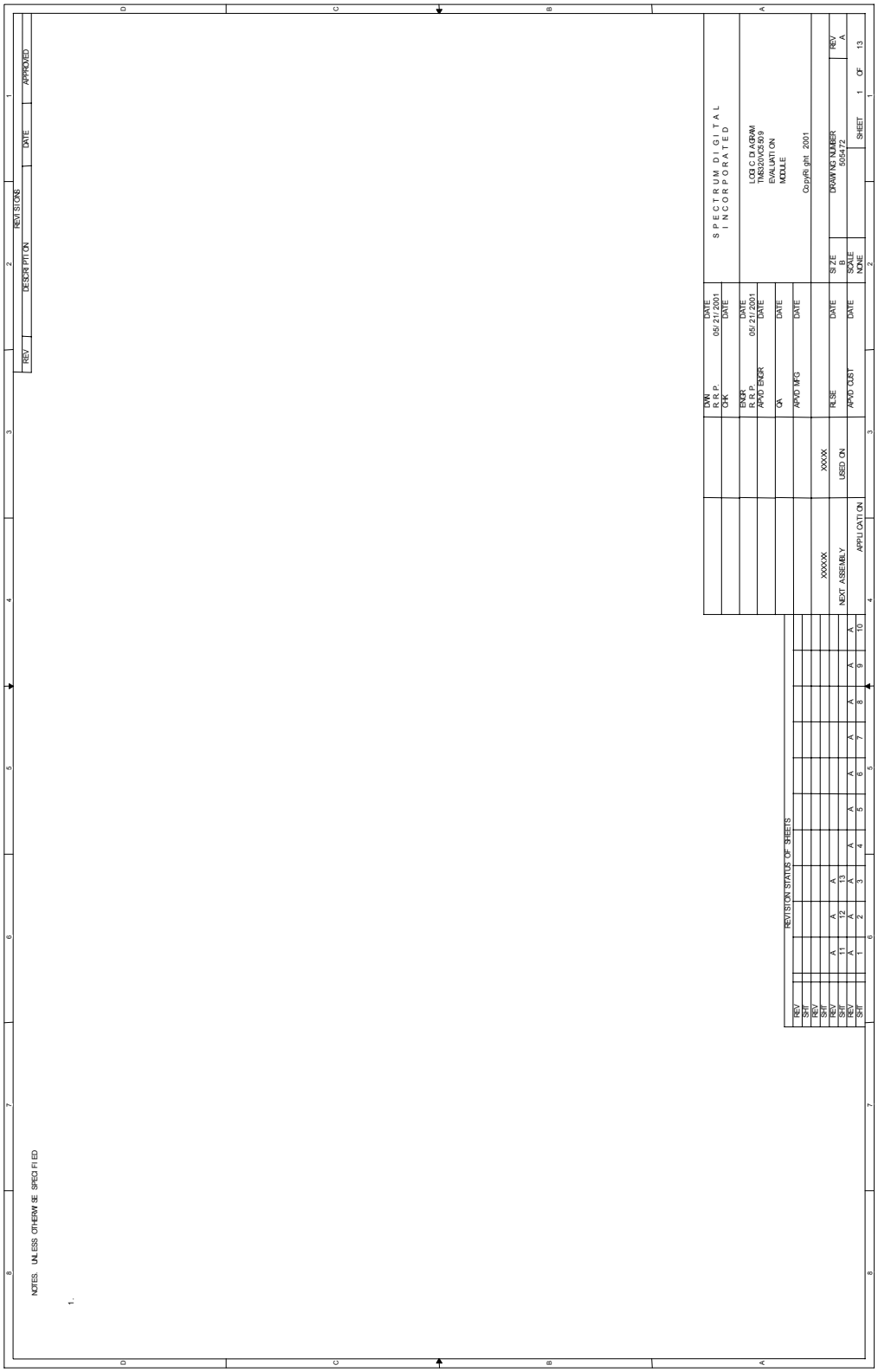
```
    -- Latch the data and address on the rising edge of iWEn
    process( iWEn, iRESETn, iCE0n, iA13, iA3, iA2, iA1, iD )
    begin
      if iRESETn = '0' then
            LcdD <= ( others => '0' );
                                LcdA0 <= '0';
          elsif iWEn'event and iWEn = '1' then
            if (      iCE0n = '0'
                                and  iA13  = '1'
                                      and  iA3   = '1'
                                      and  iA2   = '0') then
                                      LcdD <= iD;
                                      LcdA0 <= iA1;
                            end if;
          end if;
    end process;

    -- Generate a LCD Start edge.  We clear the edge once we have
    -- detected it with LcdStart.
    process( iWEn, iRESETn, iCE0n, iA13, iA3, iA2, LcdStart )
    begin
      if iRESETn = '0' or LcdStart = '1' then
   LcdRequest <= '0';
          elsif iWEn'event and iWEn = '1' then
            if (      iCE0n = '0'
                                and  iA13  = '1'
                                      and  iA3   = '1'
                                      and  iA2   = '0') then
                                      LcdRequest <= '1';
                            end if;
          end if;
    end process;

    -- Generate the LCD start request.
    -- If we have a spare flip-flop we should sync before
    -- using it.
    --
process( iRESETn, iMCLK, LcdRequest, LcdClkEn )
    begin
      if iRESETn = '0' then
   LcdStart <= '0';
          elsif iMCLK'event and iMCLK = '1' then
   if( LcdClkEn = '1' ) then
                                   LcdStart <= LcdRequest;
                                end if;
          end if;
    end process;
```

```
        -- Load the shift count with 0 on start and count up to 7
        -- The LcdSckOn signal is ON for Load/Count and OFF otherwise.
        --
  process( iRESETn, iMCLK, LcdStart, LcdClkEn )
        begin
          if iRESETn = '0' then
               LcdShiftCnt <= (others => '1');
              LcdSckOn    <= '0';
             elsif iMCLK'event and iMCLK = '1' then
        if( LcdClkEn = '1' ) then
             LcdSckOn <= '0';   -- Default
        if LcdStart = '1' then
            LcdShiftCnt <= "000";
            LcdSckOn    <= '1';
        else
            if LcdShiftCnt /= "111" then
             LcdShiftCnt <= LcdShiftCnt + "001";
             LcdSckOn  <= '1';
             end if;
             end if;
             end if;
             end if;
        end process;

        -- Mux out the data
        process( LcdShiftCnt, LcdD )
        begin
          case LcdShiftCnt( 2 downto 0 ) is
                when "111"   => LcdMuxD <= LcdD(0);
                when "110"   => LcdMuxD <= LcdD(1);
                when "101"   => LcdMuxD <= LcdD(2);
                when "100"   => LcdMuxD <= LcdD(3);
                when "011"   => LcdMuxD <= LcdD(4);
                when "010"   => LcdMuxD <= LcdD(5);
                when "001"   => LcdMuxD <= LcdD(6);
                when others  => LcdMuxD <= LcdD(7);
    end case;
        end process;

        oLCDSI   <= LcdMuxD;
        oLCDSCK  <= MclkDiv(1) when LcdSckOn = '1' else '1';
        oLCDA0   <= LcdA0;
        oLCDBUSY <= '0' when (    LcdRequest  = '1'
                          or LcdStart    = '1'
                                    or LcdSckOn    = '1' ) else 'Z';

end behavior_evm5509;
```

Appendix B

TMS320VC5509 EVM Schematics

This appendix contains the schematics for the TMS320VC5509 EVM. The schematics were drawn in ORCAD.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DATE
APPROVED
REV
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TMS320VC5509
EVALUATION
MODULE
Copyright 2001
DRAWING NUMBER
SD6472
REV
A
SIZE
B
SCALE
NONE
SHEET 1 OF 13
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R.R.P.
05/21/2001
CHK
ENGR
R.R.P.
05/21/2001
APVD ENGR
QA
APVD MFG
APVD CUST
DATE
XXXXX
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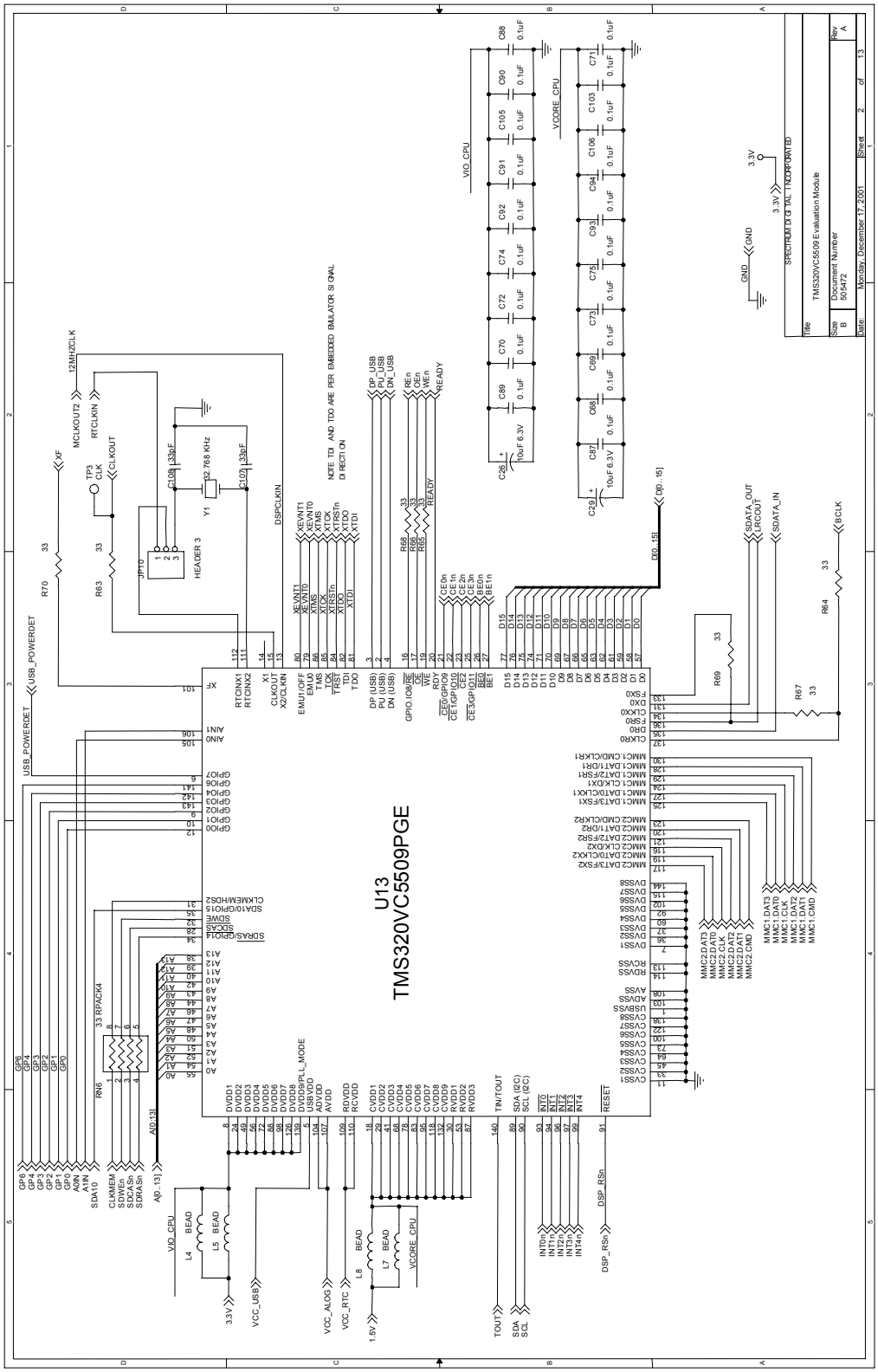
USED ON
NEXT ASSEMBLY
APPLICATION
REVISION STATUS OF SHEETS


U13
TMS320VC5509PGE
TMS320VC5509 Evaluation Module
Document Number
505472
Monday, December 17, 2001
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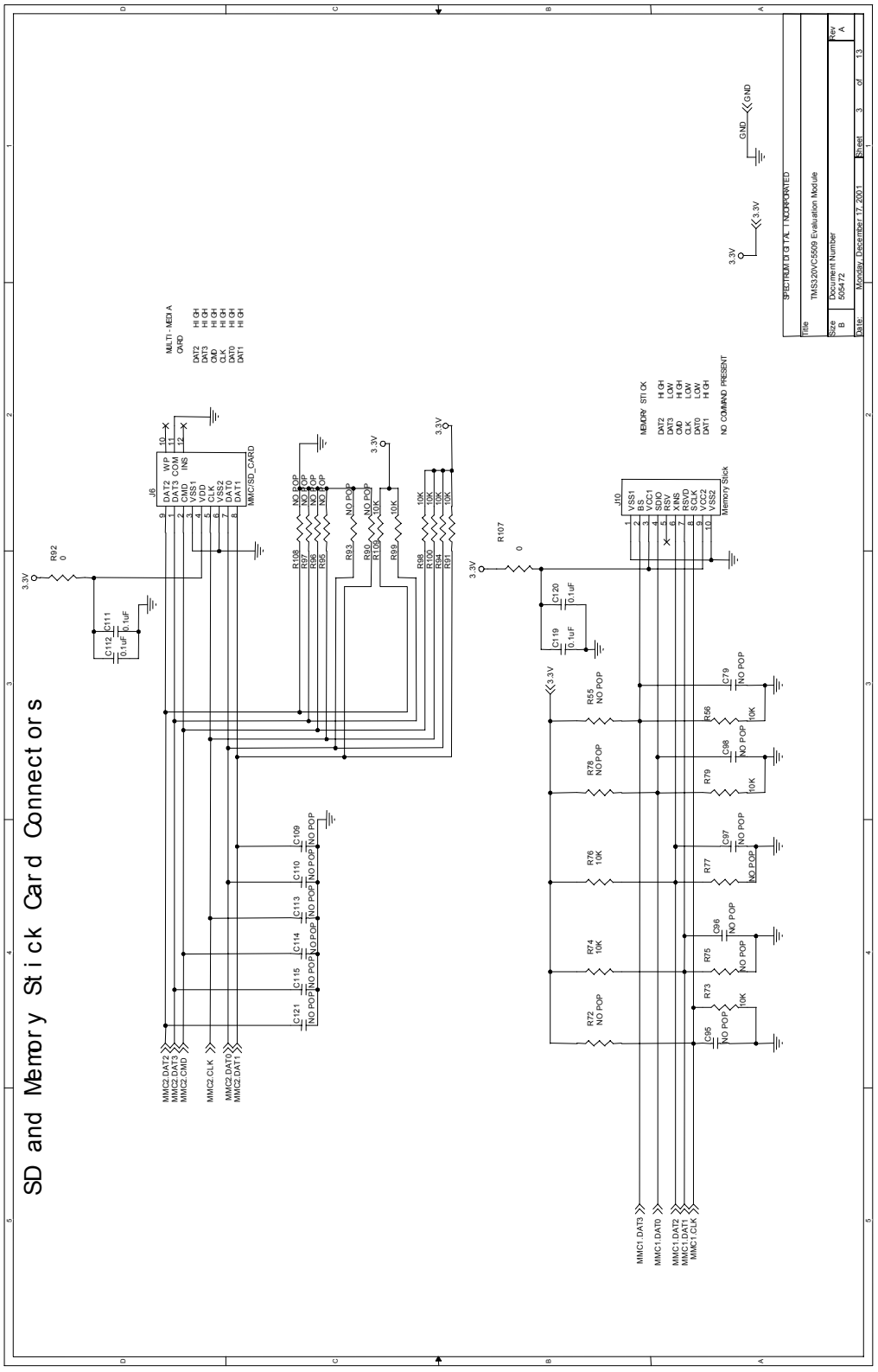
MCLKOUT2
RTCLKIN
CLKOUT
DSPCLKIN
32.768 KHz
USB_POWERDET
VIO_CPU
VCORE_CPU
VCC_USB
VCC_ALOG
VCC_RTC
1.5V
3.3V
GND
TOUT
SDA
SCL
DSP_RSn
SDATA_OUT
SDATA_IN
IRCOUT
BCLK
NOTE: TDI AND TDO ARE FOR EMBEDDED EMULATOR SIGNAL DIRECTION ON
MMC1.DAT3
MMC1.DAT0
MMC1.CLK
MMC1.DAT2
MMC1.DAT1
MMC1.CMD
MMC2.DAT3
MMC2.DAT0
MMC2.CLK
MMC2.DAT2
MMC2.DAT1
MMC2.CMD


SD and Memory Stick Card Connectors
TMS320VC5509 Evaluation Module
Document Number
505472
Monday, December 17, 2001
MMC/SD_CARD
Memory Stick
MEMORY STICK
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MMC2.DAT2
MMC2.DAT3
MMC2.CMD
MMC2.CLK
MMC2.DAT0
MMC2.DAT1
MMC1.DAT3
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MMC1.DAT2
MMC1.DAT1
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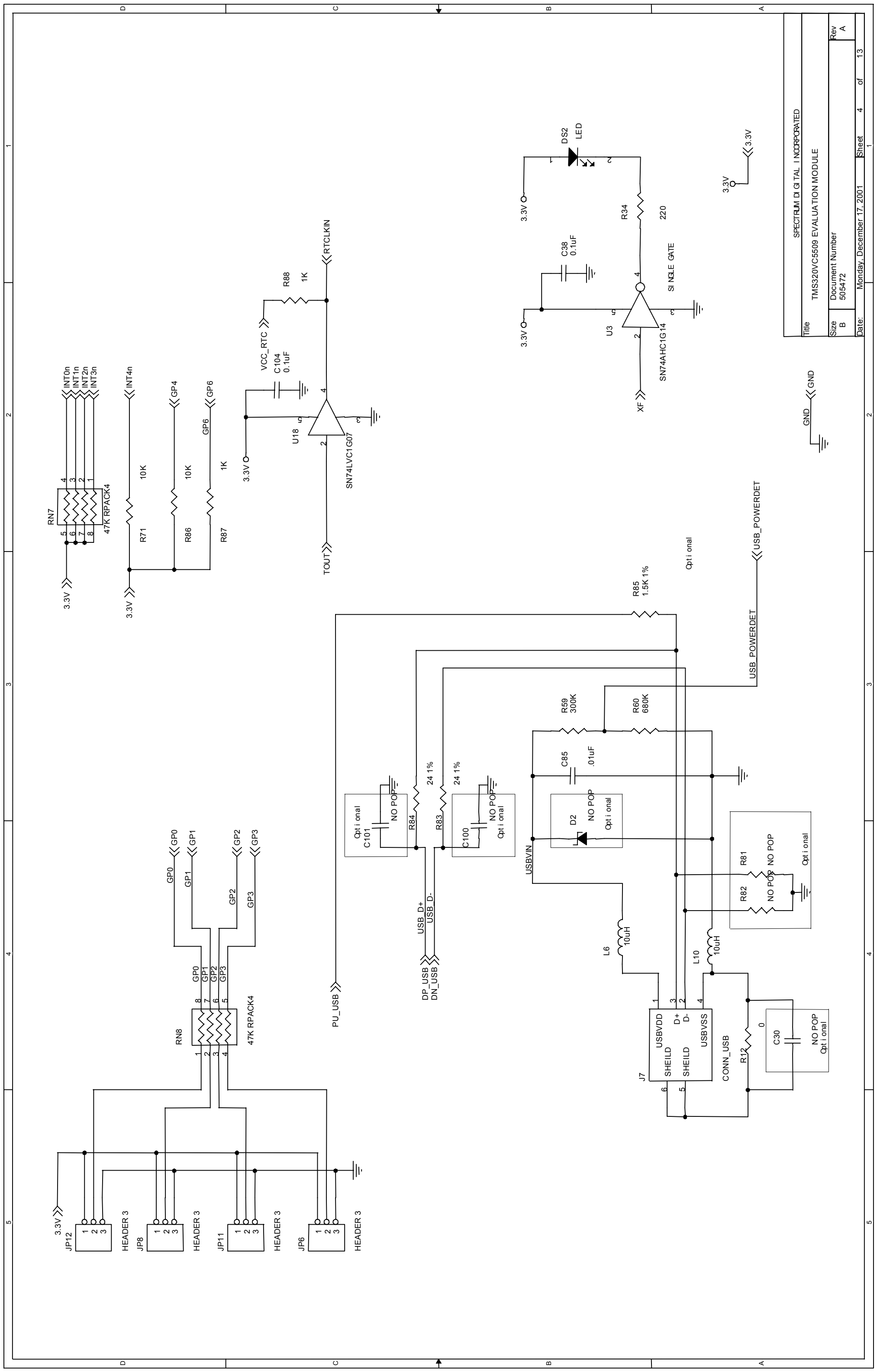
3.3V
GND
NO POP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Size
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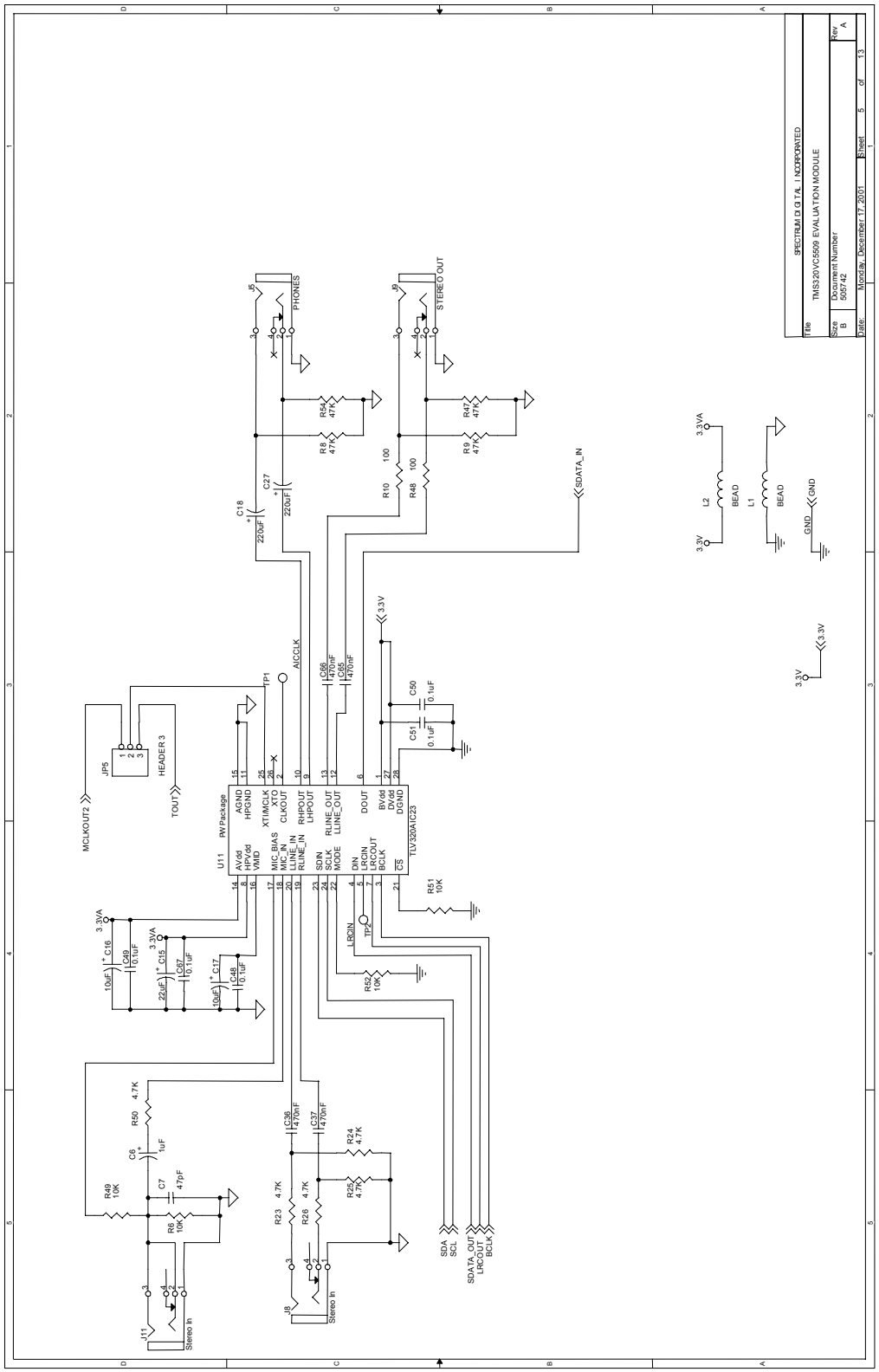
Document Number
505472
Rev
A
Date: Monday, December 17, 2001
Sheet 4 of 13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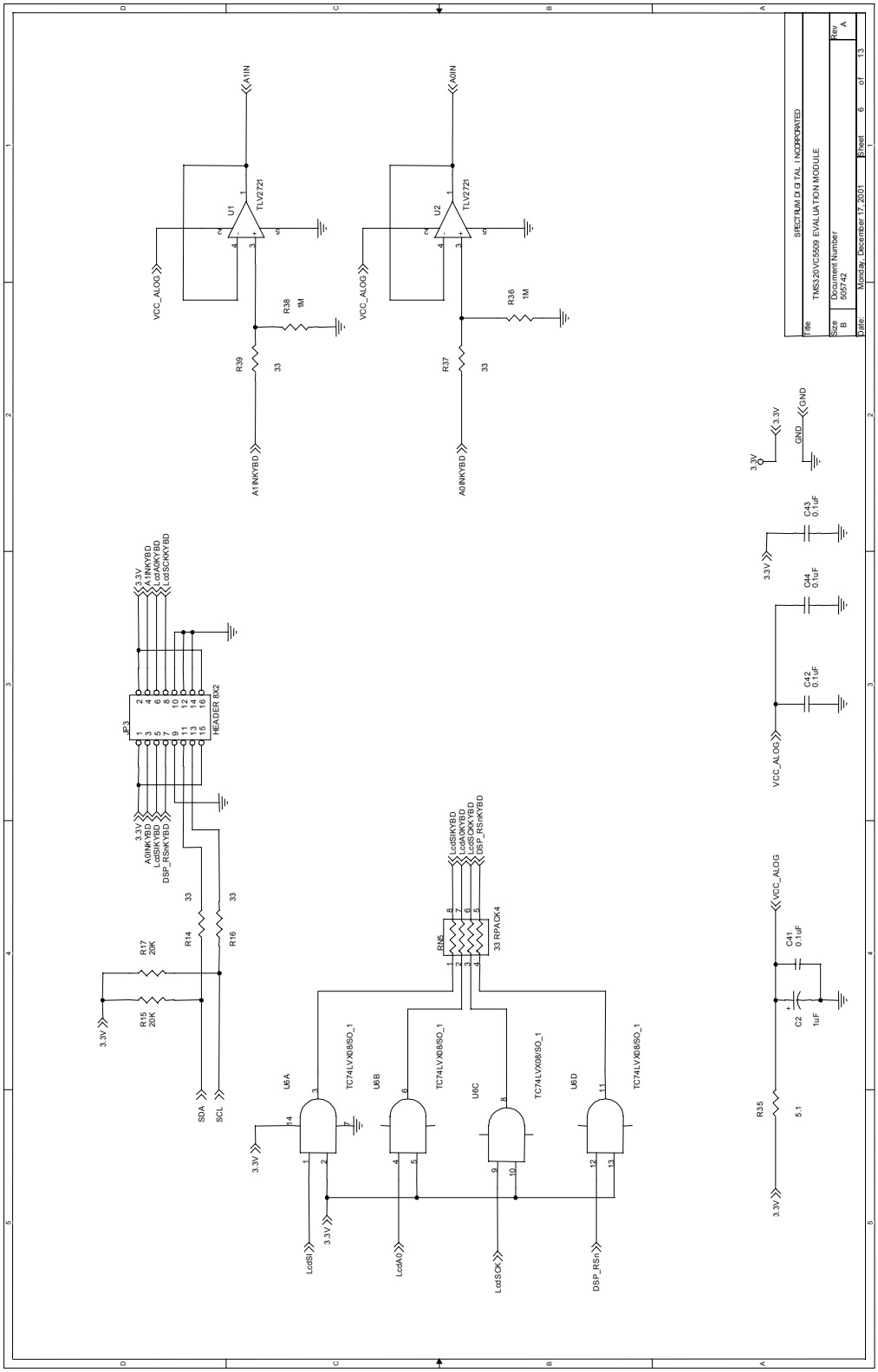
Size
B
Document Number
505742
Rev
A
Date:
Monday, December 17, 2001
Sheet
5
of
13
PHONES
STEREO OUT
HEADER 3
TLV320AIC23
PW Package
Stereo In
Stereo In
SDATA_IN
AICCLK
MCLKOUT2
TOUT
LRCIN
SDA
SCL
SDATA_OUT
LRCOUT
BCLK
3.3V
3.3VA
GND
BEAD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Size B
Document Number 505742
Rev A
Date: Monday, December 17, 2001
Sheet 6 of 13
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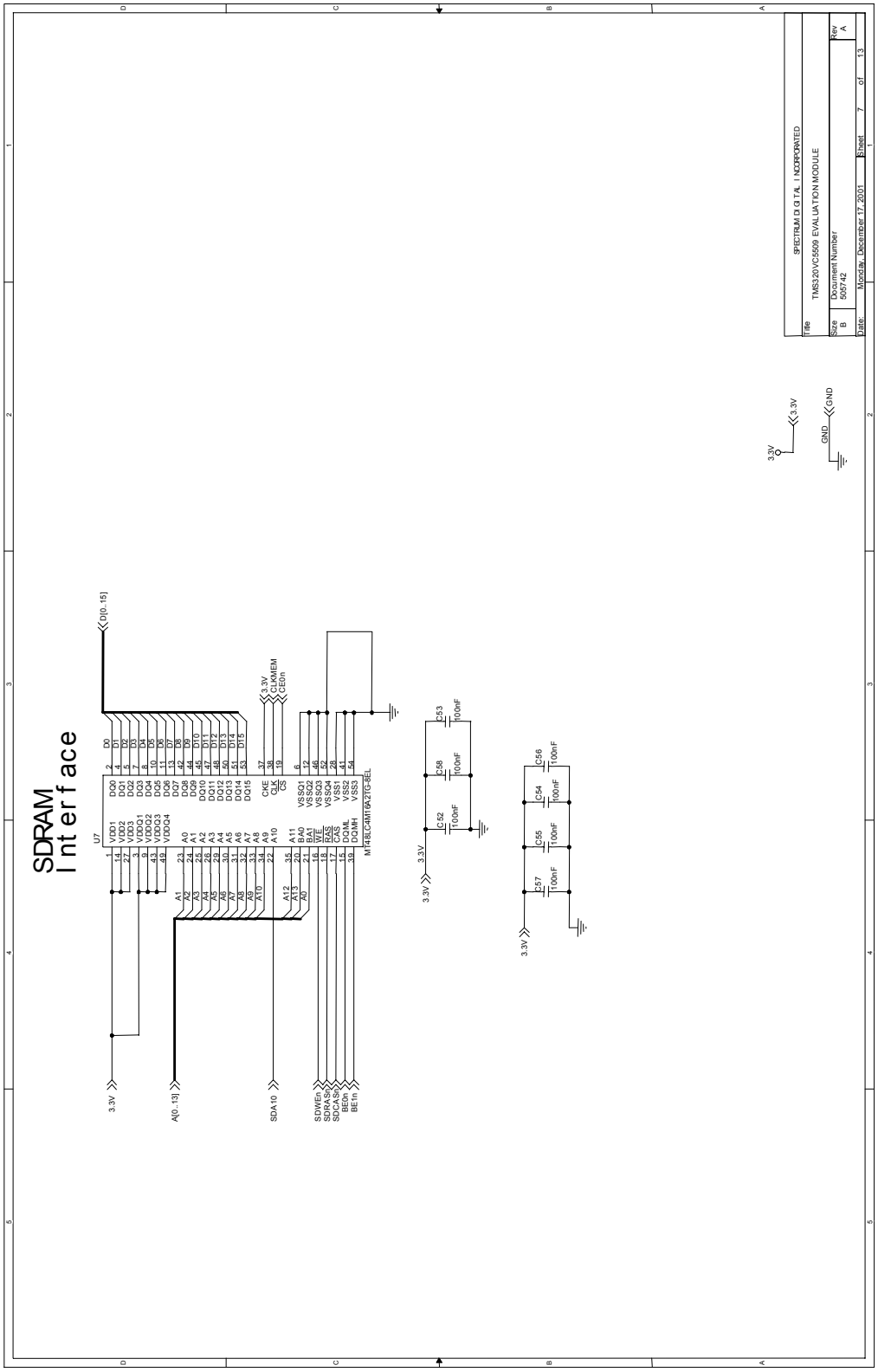
A0IN
U1
U2
TLV2721
VCC_ALOG
R38 9M
R36 1M
R39 33
R37 33
A1INKYBD
A0INKYBD
3.3V
GND
C43 0.1uF
C44 0.1uF
C42 0.1uF
C41 0.1uF
C2 1uF
R35 5.1
JP3
HEADER 8X2
LcdA0KYBD
LcdSCKKYBD
DSP_RShKYBD
LcdSIKYBD
R17 20K
R15 20K
R14 33
R16 33
SDA
SCL
RN5
33 RPACK4
U6A
U6B
U6C
U6D
TC74LVX08/SO_1
LcdSI
LcdA0
LcdSCK
DSP_RSh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TMS320VC5509 EVALUATION MODULE
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GND
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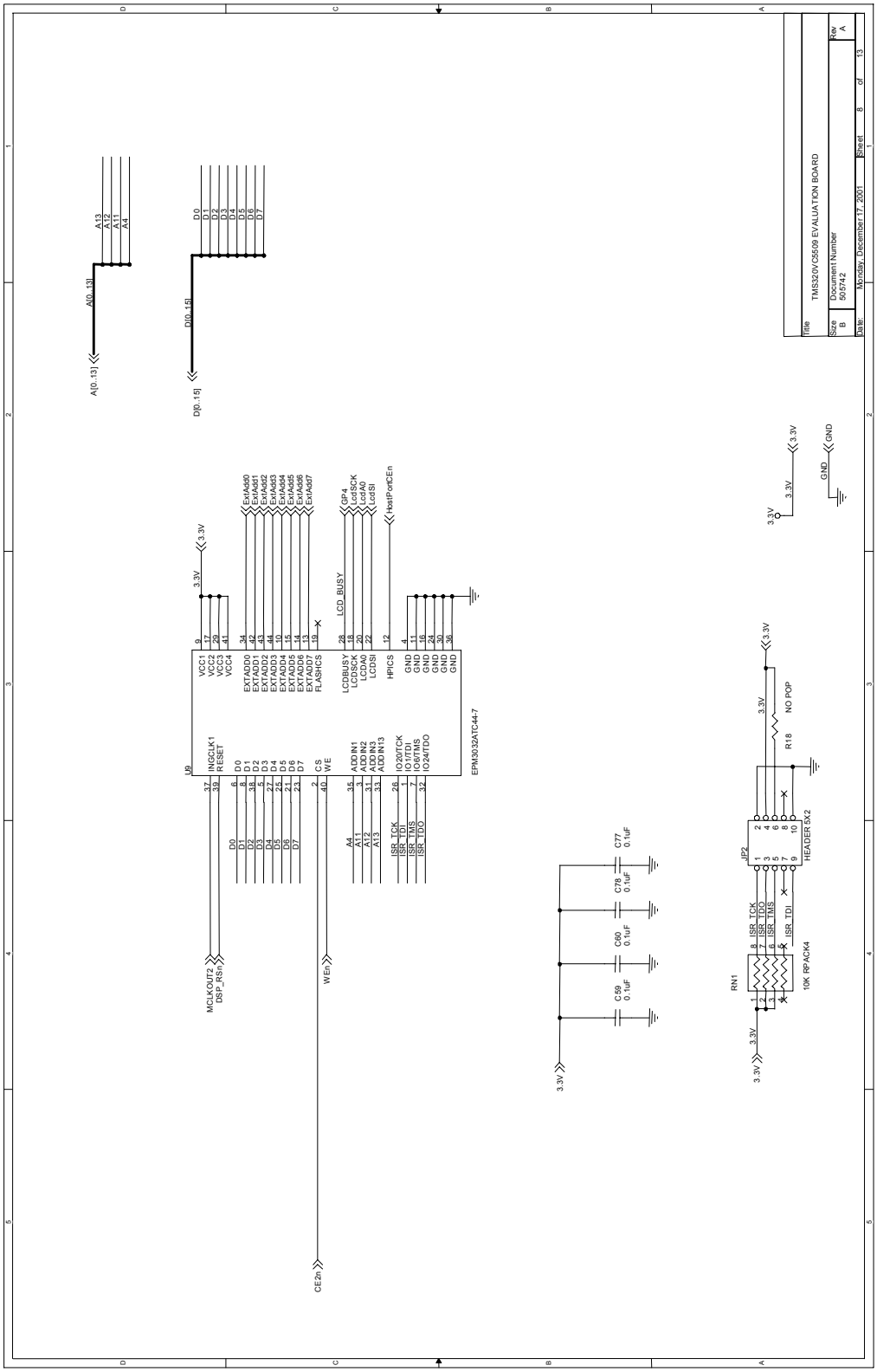
SDWEn
SDRASn
SDCASn
BE1n
BE0n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Monday, December 17, 2001
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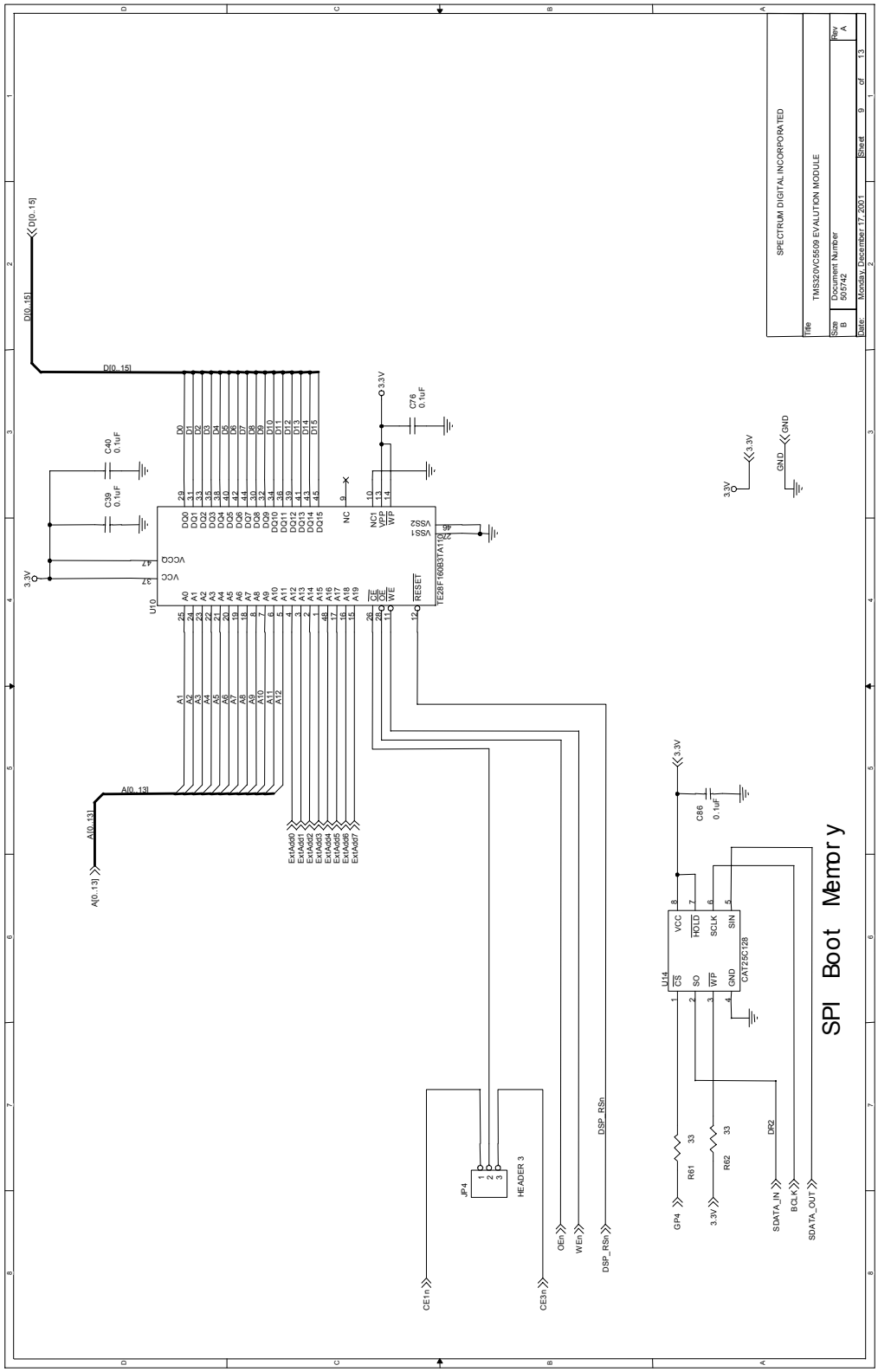
JP2
HEADER 5X2
RN1
10K RPACK4
R18
NO POP
C59 0.1uF
C60 0.1uF
C78 0.1uF
C77 0.1uF
A[0..13]
D[0..15]
MCLKOUT2
DSP_RSn
WEn
CE2n
HostPortCEn
LCD_BUSY
3.3V
GND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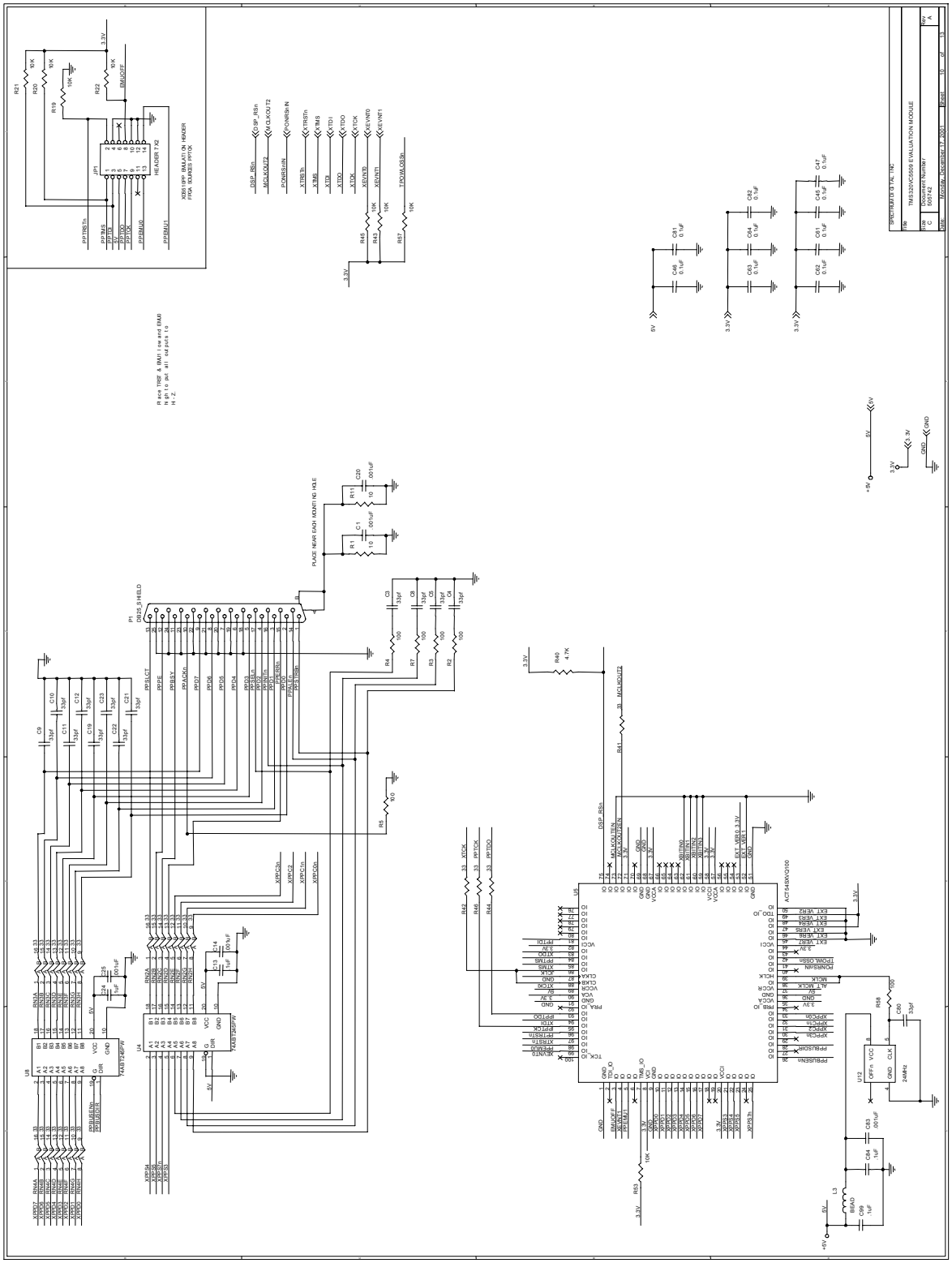
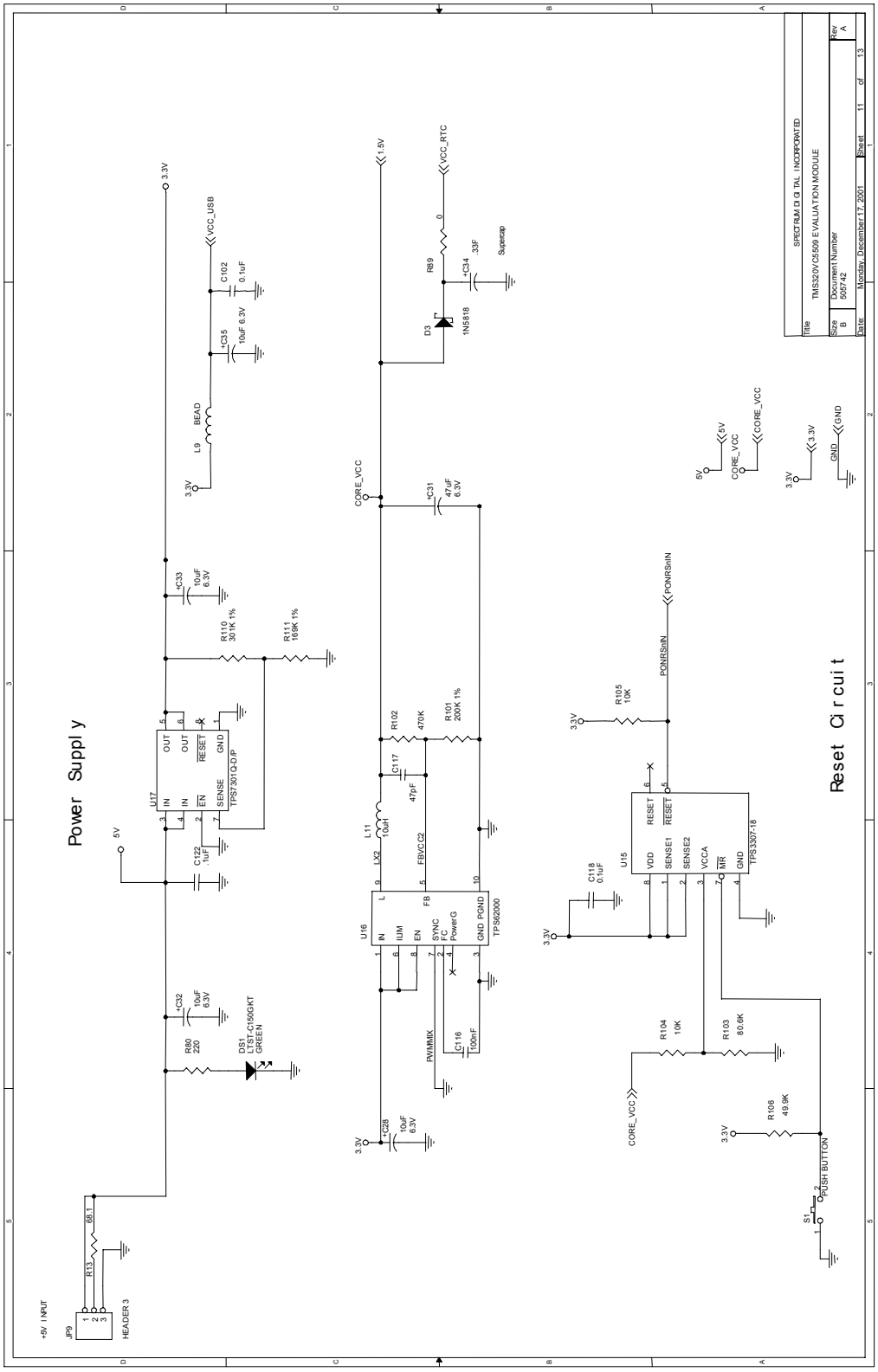
TMS320VC5509 EVALUTION MODULE
Document Number
505742
Monday, December 17, 2001
SPI Boot Memory
U10
U14
JP4
HEADER 3
C40
C39
C76
C86
R61
R62
D[0..15]
A[0..13]
3.3V
GND
CE1n
CE3n
OEn
WEn
DSP_RSn
SDATA_IN
BCLK
SDATA_OUT
GP4

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Reset Circuit
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TMS320VC5509 EVALUATION MODULE
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JP9
HEADER 3
R13
68.1
U17
TPS73301QDRP
U16
TPS62000
U15
TPS3307-18
L11
10uH
L9
BEAD
D3
1N5818
DS1
LTST-C150GKT
GREEN
R80
220
R89
0
R110
301K 1%
R111
169K 1%
R102
470K
R101
200K 1%
R105
10K
R104
10K
R103
80.6K
R106
49.9K
C102
0.1uF
C117
47pF
C118
0.1uF
C122
1uF
C116
100nF
+C31
47uF 6.3V
+C32
10uF 6.3V
+C33
10uF 6.3V
+C34
.33F
Supercap
+C35
10uF 6.3V
+C28
10uF 6.3V
S1
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5V
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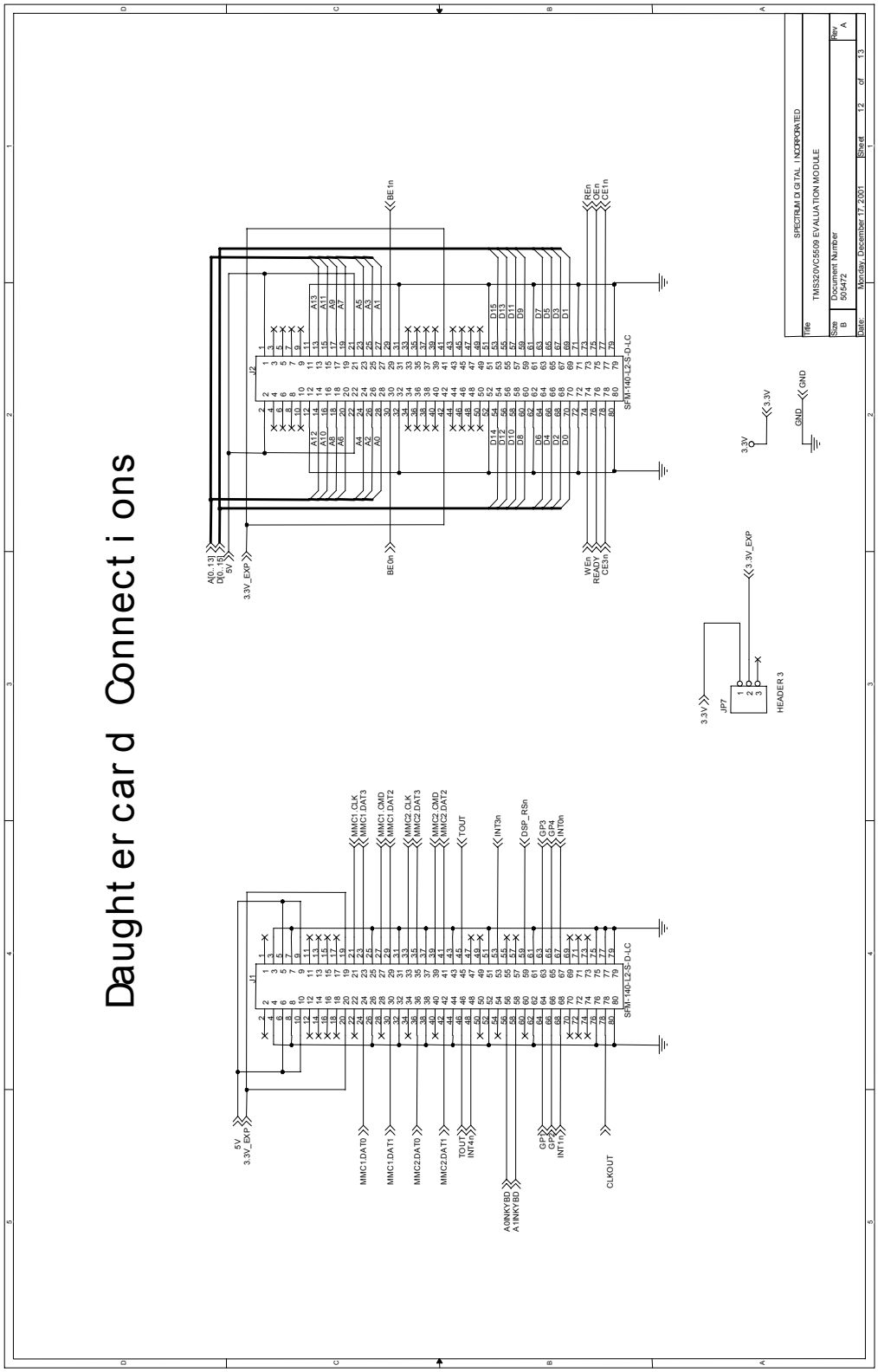
VCC_RTC
CORE_VCC
PONRSnIN
PWMMIX
GND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GND
5V
R27
10K
R28
R29
R30
R32
R33
R34
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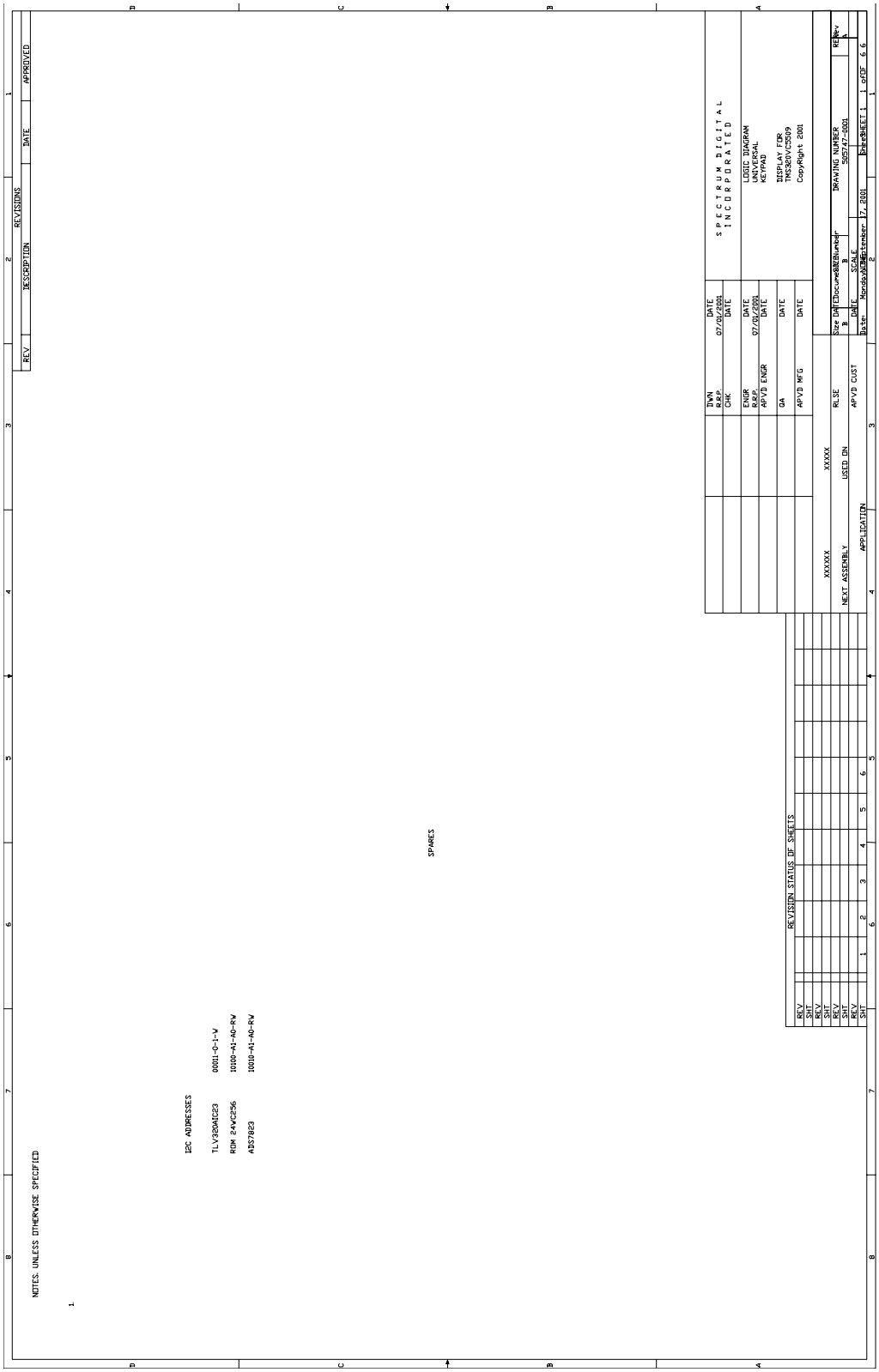
Appendix C

Universal Display/Keypad Module Schematics

This appendix contains the schematics for the Universal Display/Keypad module that is used with the TMS320VC5509 EVM. The schematics were drawn in ORCAD.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ROM 24WC256 1010-A1-A0-RW
ADS7823 1001-A1-A0-RW
SPARES
REVISION STATUS OF SHEETS
REV
SHT
SPECTRUM DIGITAL INCORPORATED
DRAWING NUMBER
LOGIC DIAGRAM
UNIVERSAL
KEYPAD
DISPLAY FOR
TMS320VC5509
CopyRight 2001
SCALE
SHEET 1 OF 1
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USED ON
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APVD CUST
APVD MFG
RLSE
DVN
CHK
ENGR
APVB ENGR
QA
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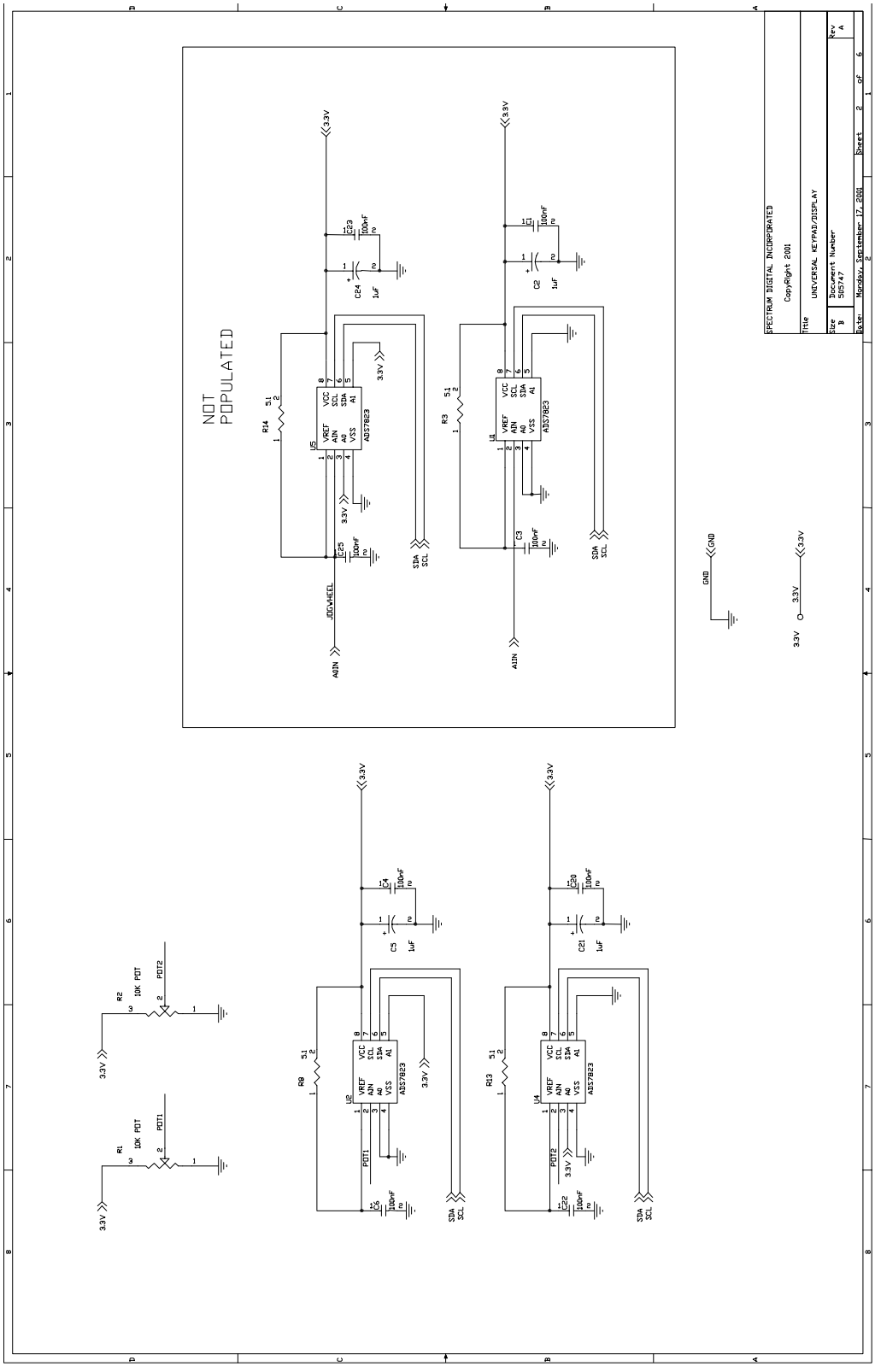
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Sheet 2 of 6
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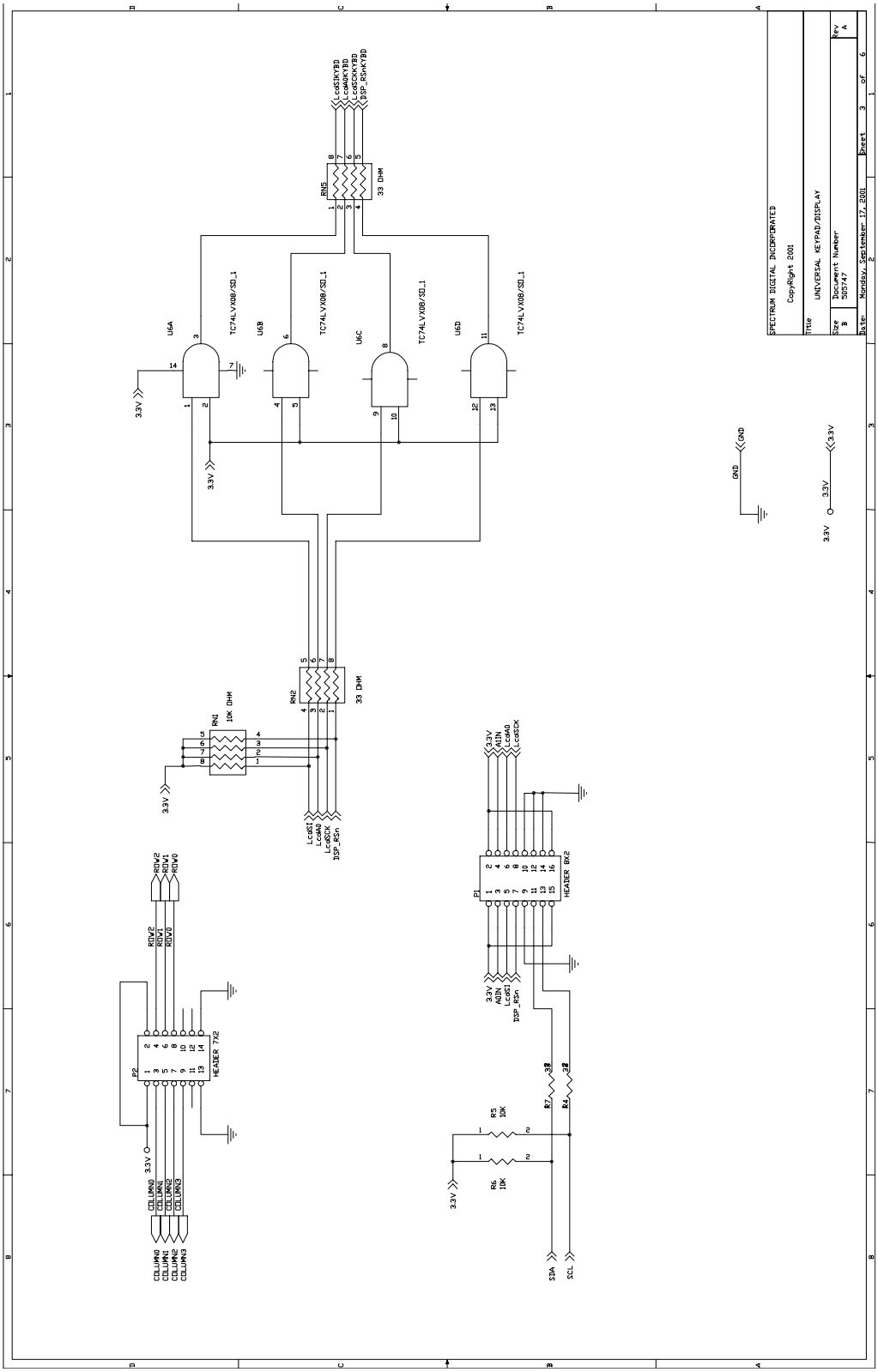
GND
SDA
SCL
AIN
JOGWHEEL
PDT1
PDT2
ADS7823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Sheet
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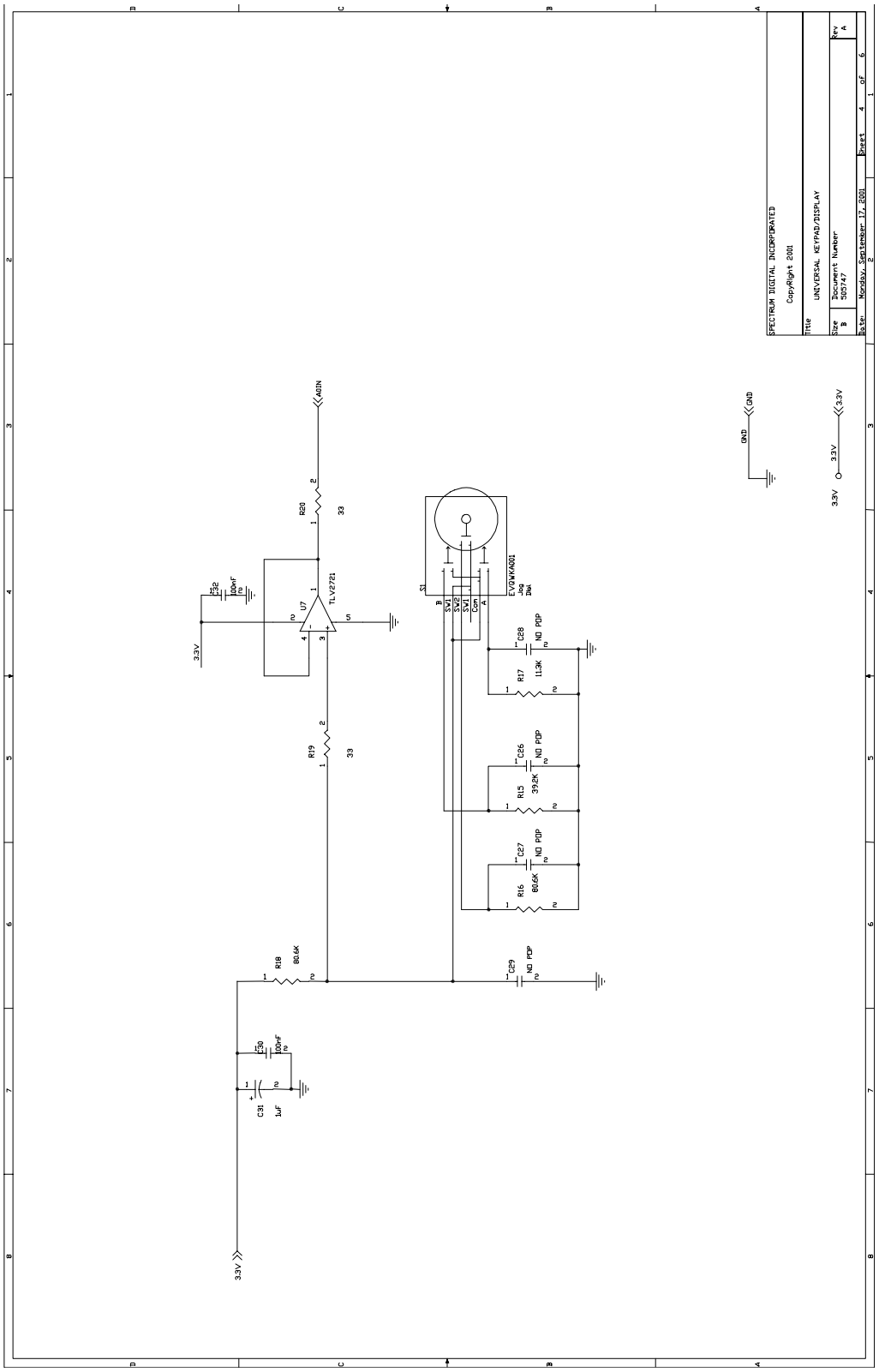
of
6
U6A
U6B
U6C
U6D
TC74LVX08/SL_1
RN5
33 OHM
RN2
33 OHM
RN1
10K OHM
P2
HEADER 7X2
P1
HEADER 8X2
R5
10K
R6
10K
R7
33
R4
33
3.3V
GND
COLUMN0
COLUMN1
COLUMN2
COLUMN3
ROW2
ROW1
ROW0
SDA
SCL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Sheet
4
of
6
AOIN
R20
33
C32
10nF
U7
TLV2721
3.3V
S1
EVQWKA001
SW3
SW2
SW1
Com
C28
NO POP
R17
113K
R19
33
C26
NO POP
R15
39.2K
C27
NO POP
R16
80.6K
R18
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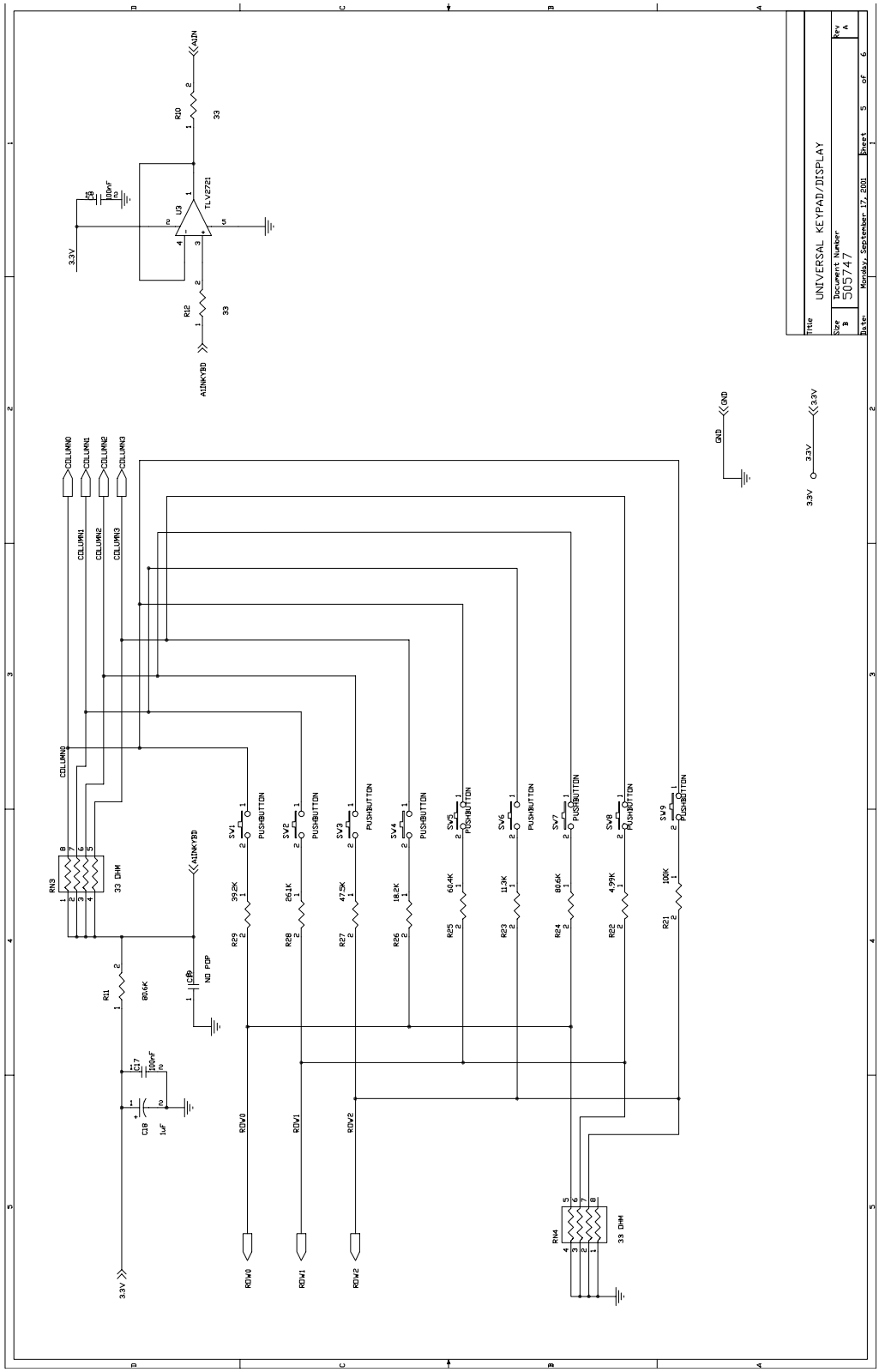
3.3V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COLUMN2
COLUMN3
ROW0
ROW1
ROW2
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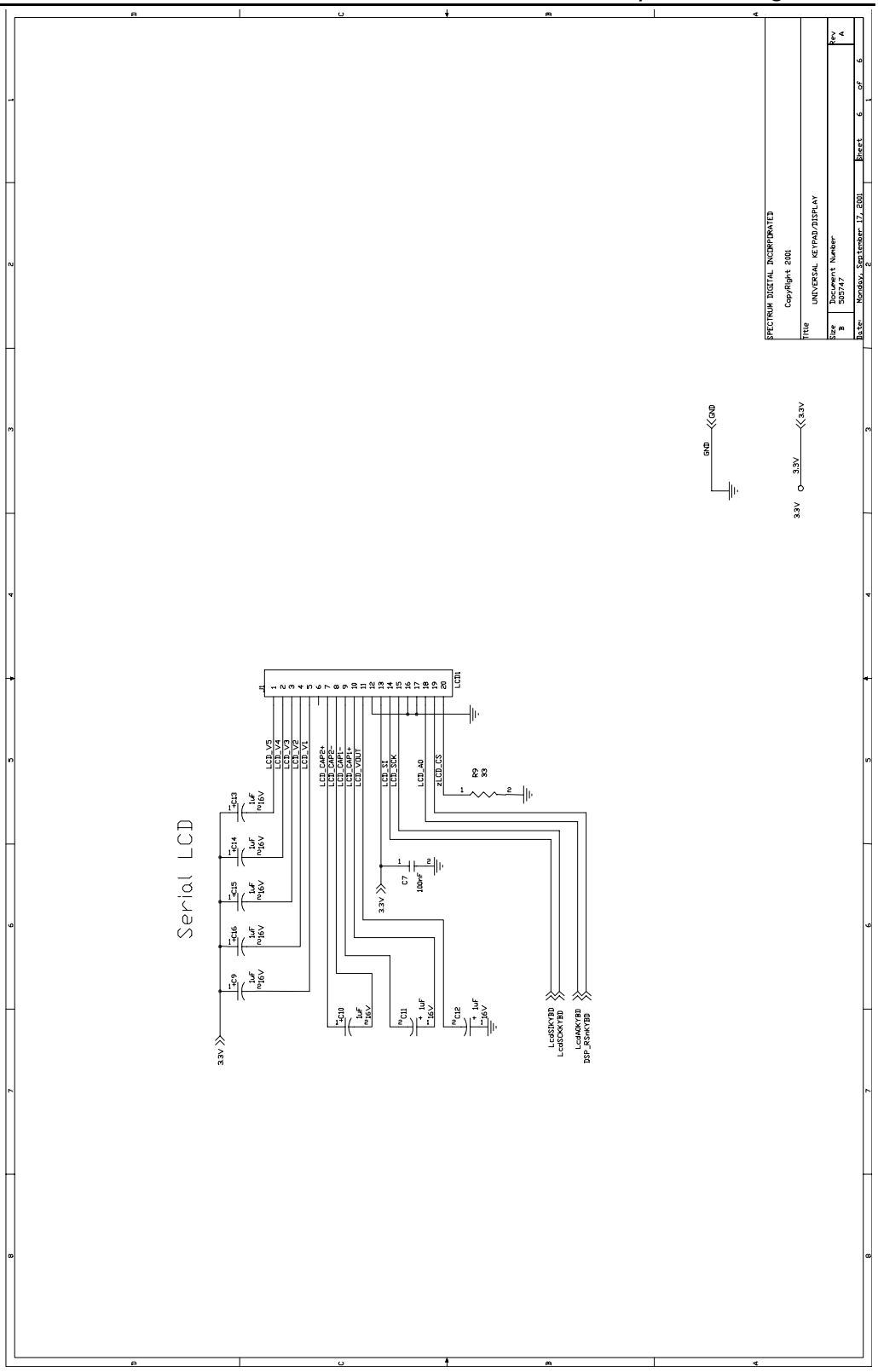
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C7
100nF
C9
C10
C11
C12
C13
C14
C15
C16
3.3V
GND
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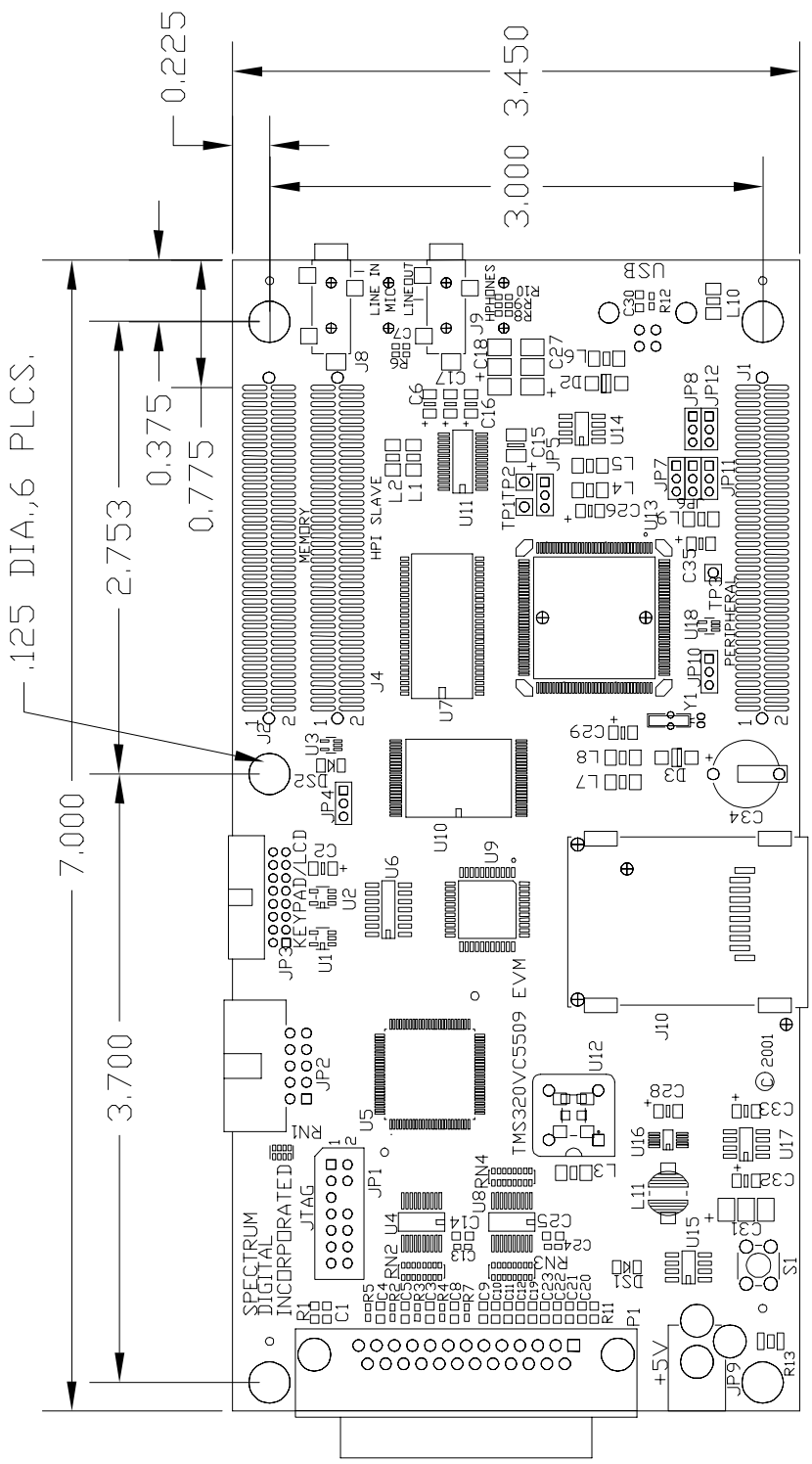
LCD_V4
LCD_V3
LCD_V2
LCD_V1
LCD_CAP2+
LCD_CAP2-
LCD_CAP1-
LCD_CAP1+
LCD_VOUT
LCD_SI
LCD_SCK
LCD_A0
2LCD_CS
LcdSIKYBD
LcdSCKKYBD
LcdA0KYBD
DSP_RSHKYBD

Appendix D

EVM320VC5509 Mechanical Information

This appendix contains the mechanical information about the EVM320VC5509 produced by Spectrum Digital.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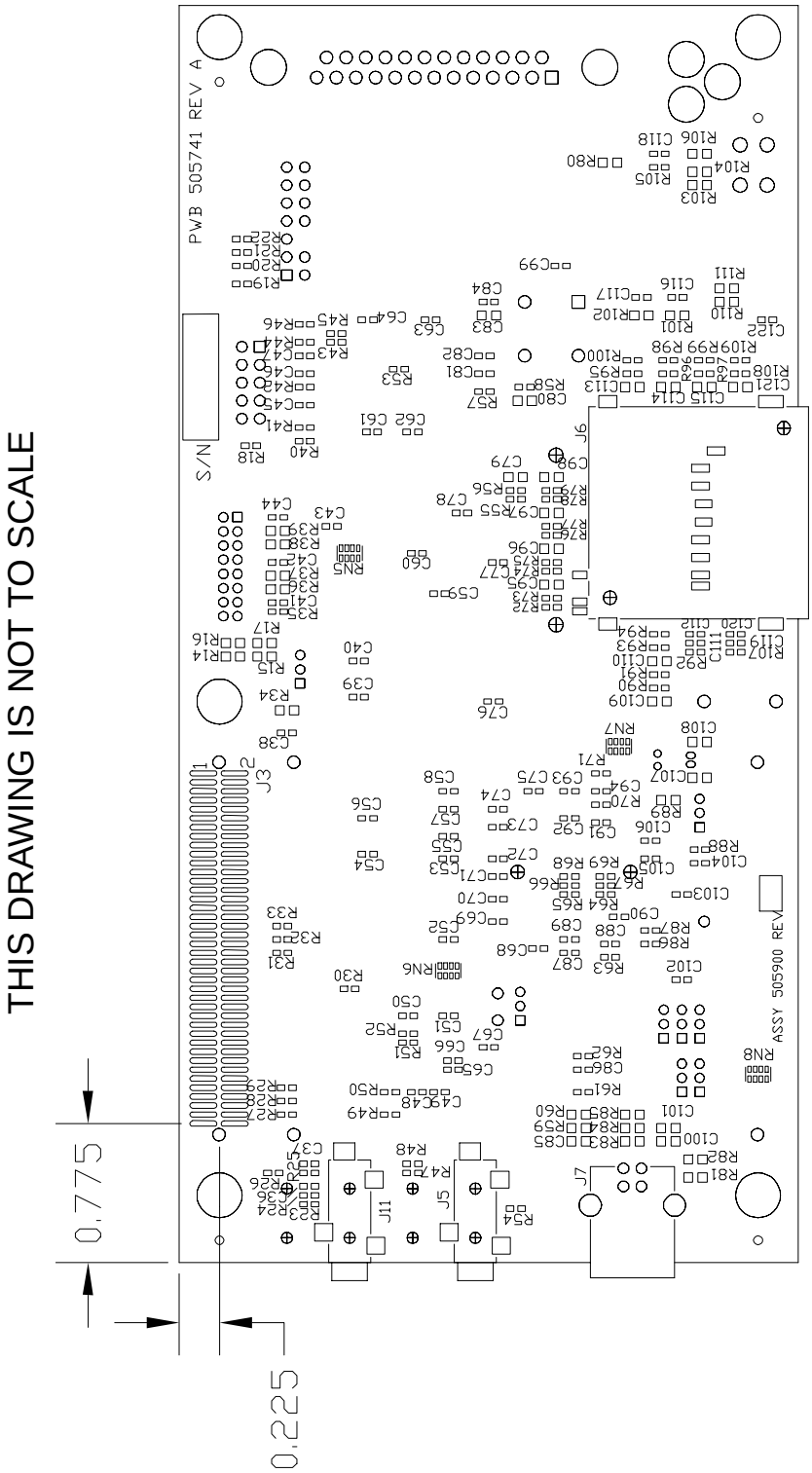
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