SPECTRUM DIGITAL INCORPORATED

TMS320VC5509A EVM PLUS

Technical Reference

2004 ***DSP Development Systems***

TMS320VC5509A EVM PLUS
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5509A Evaluation Module (EVM PLUS). The EVM PLUS is based on the Texas Instruments TMS320VC5509A Digital Signal Processor.

The TMS320VC5509A EVM PLUS is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5509A DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5509A will sometimes be referred to as the C55XX.

The TMS320VC5509A EVM PLUS will sometimes be referred to as the EVM PLUS.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release

Table 2: Manual History

Revision	History
A	Alpha Release

Chapter 1

Introduction to the TMS320VC5509A EVM PLUS

Chapter One provides a description of the TMS320VC5509A EVM PLUS along with the key features and a block diagram of the circuit board.

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1.0 Key Features

The 5509A EVM PLUS is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The EVM PLUS also serves as a hardware reference design for the TMS320VC5509A DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

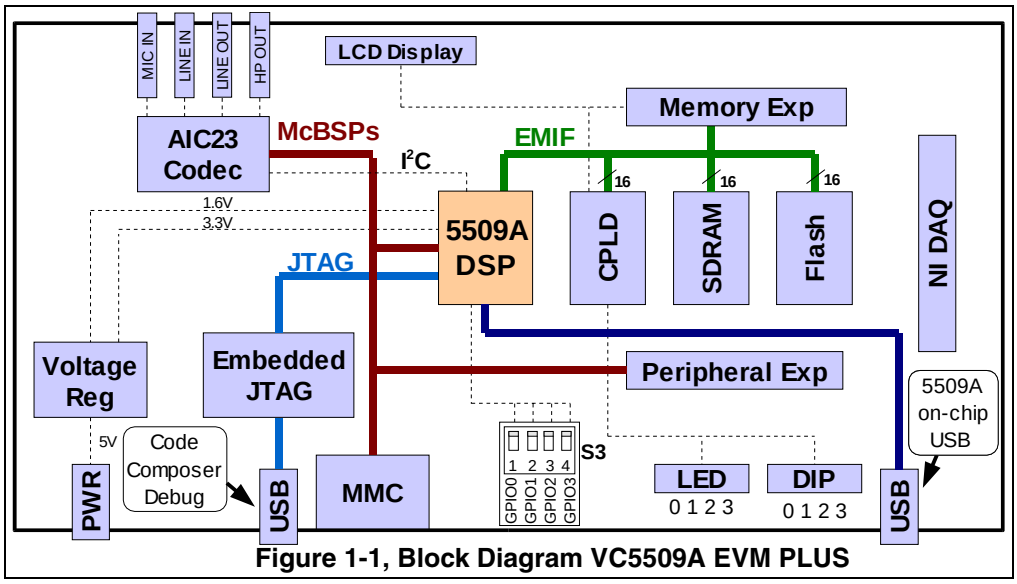

Figure 1-1, Block Diagram VC5509A EVM PLUS

The EVM PLUS comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320VC5509A-GHH DSP
- Selectable core voltages (1.2V, 1.4V, 1.6V)
- Power test points and current shunts
- An AIC23B stereo codec
- 8 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- User USB port via VC5509A
- Software board configuration through registers implemented in CPLD
- Switch selectable boot options

- 128 x 64 display and position keypad
- Standard expansion connectors for daughter card use
- National Instruments interface
- JTAG emulation through on-board JTAG emulator with USB host interface or external emulator
- MMC card interface
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320VC5509A EVM PLUS

The DSP interfaces to external SDRAM, Flash memory and an expansion memory interface connector through its 16-bit External Memory Interface (EMIF). The SDRAM accesses are in 16-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23B codec allows the DSP to transmit and receive analog signals. I^2C is used for the codec control interface and McBSP0 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors.

McBSP2 interfaces to a MultiMedia card. This allows the DSP a way to store off data for video and audio applications. McBSP1 and McBSP2 are routed to the expansion connectors via software configuration registers in the CPLD

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The EVM PLUS includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers. A wake-up push button allows the DSP to be interrupted, to “wake up” the DSP when it is in sleep or idle mode.

An included 5V external power supply is used to power the board. On-board voltage regulators provide the 1.6V to 1.2V DSP core voltage, 3.3V digital and 3.3V analog voltages. A voltage supervisor monitors the internally generated voltage, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

Code Composer communicates with the EVM PLUS through an embedded JTAG emulator with a USB host interface. The EVM PLUS can also be used with an external emulator through the external JTAG connector.

1.3 Basic Operation

The EVM PLUS is designed to work with TI's Code Composer Studio (CCS) development environment. Code Composer communicates with the board through the on-board JTAG emulator, or an external emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The EVM PLUS must be fully connected to launch Code Composer Studio.

1) Connect the included power supply to the EVM PLUS.

2) Connect the EVM PLUS to your PC with a mini USB cable (also included).

3) Set up Code Composer Studio

4) Launch Code Composer from its icon on your desktop.

Detailed information about the CCS including a tutorial, examples and reference material is available in the EVM PLUS's help file. You can access the help file through Code Composer's help menu.

1.4 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5509A is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 21 address bits are driven on the EMIF as address lines while the top 3 are decoded and driven as the chip enable for that particular region.

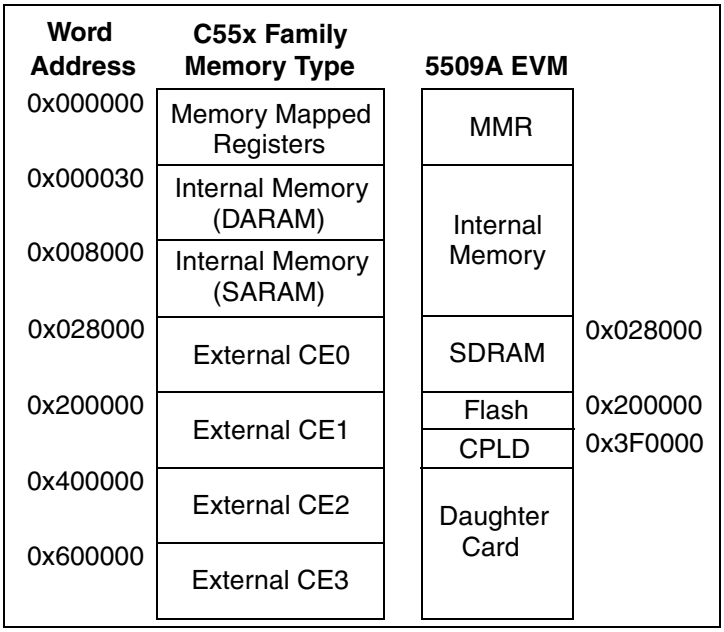

Figure 1-2, Memory Map, VC5509A EVM PLUS

The figure above shows a generic memory space map for a C55x family processor and a second map specific to the components on a 5509A EVM PLUS. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the lower section and the CPLD in the upper section of memory.

Internal memory on the 5509A starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM and a larger amount of internal SARAM. DARAM stands for Dual-Access RAM and is differentiated from SARAM (Single-Access RAM) in that two concurrent memory operations can be performed on the same block rather than one.

Internal memory is divided into blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. DARAM blocks are the most precious because their dual-ported nature allows a higher rate of operation. There are 32K words of DARAM and 96K words of SARAM on a 5509A for a total of 128K words of internal memory.

1.5 Boot Mode Settings

The 5509A EVM PLUS has 4 position switch that define the DSP's boot configuration at reset. The figure below shows this switch.

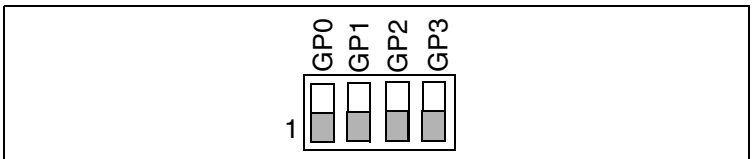

Figure 1-3, JP4, DSP Boot Configuration - Default Setting

The switches drive signals that directly correspond to the input on one of the DSP's GP[3-0] configuration pins. If the switch is on, the signal is driven to a logic 0. If the switch is off, the signal is driven to a logic 1.

The 5509A can boot from asynchronous memory mapped in CE1 (Flash on the 5509A EVM PLUS board), serial EEPROM's connected to McBSP0 or a standard serial port on McBSP0. To boot from a particular device you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumpers and power cycle the board, the 5509A will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5509A usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins. In the special case where BOOTM[3:0] are all 0, the internal ROM is not active and execution will begin from external memory at the reset vector (0xFFFF00).

Table 1: VC5509A EVM PLUS Boot Load Options

GPIO0	GPIO1	GPIO2	GPIO3	BOOT MODE PROCESS	SUPPORTED ON EVM
0	0	0	0	Reserved	No
0	1	0	0	Serial SPI EPROM boot (24 bit address) via McBSP0	No
0	0	1	0	USB	Yes
0	1	1	0	I^2C EEPROM (7 bit address)	No
0	0	0	1	Reserved	No
0	1	0	1	HPI - multiplexed mode	No
0	0	1	1	HPI - non multiplexed mode	No
0	1	1	1	Reserved	No
1	0	0	0	Execute from 16-bit wide asychronous memory (on CE1- space)	Yes
1	1		0	Serial SPI EPROM boot (16 bit address) via McBSP0	Yes
1	0	1	0	8-bit wide asychronous memory (on CE1- space)	No
1	1	1	0	16-bit wide asychronous memory (on CE1- space)	Yes *
1	0	0	1	Reserved	No
1	1	0	1	Reserved	No
1	0	1	1	Standard serial boot from McBSP0 (16-bit data)	No
1	1	1	1	Standard serial boot from McBSP0 (8-bit data)	No

* default on EVM

1.6 Power Supply

The EVM PLUS operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.6V and +3.3V. The +1.6V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm. barrel-type plug.

The core voltage on the EVM PLUS is selectable based on the output of GPIO5 and GPIO6 or CPLD control registers. If GPIO5 and GPIO6 are high or configured as an input the core voltage will remain at +1.6V. If GPIO5 and GPIO6 are driven low the voltage will drop to +1.2V. The table below shows the 3 core voltage levels available on the VC5509 EVM PLUS.

Table 2: Core Voltage Level Select

GPIO6	GPIO5	Core Voltage Selected
0	0	1.2V
0	1	1.4V
1	0	1.4V
1	1	1.6V

There are three power test points on the EVM PLUS at JP2, JP3 and JP6. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. JP6 allows measurement of DSP I/O pins. To measure the current passing connect the pins with a voltage measuring device. A current shunt is also supplied to amplify this voltage. This allows voltage meters to more accurately track current changes.

The EVM PLUS also provides +3.3V for the daughter card. It is also possible to provide the daughter card with +12V and -12V when the external power connector is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320VC5509A EVM PLUS.

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2.1 CPLD (Programmable Logic)

The ’C5509A EVM PLUS uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- 11 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the 5509A EVM PLUS. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5509A can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the 5509A EVM PLUS, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the 5509A EVM PLUS). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the 5509A EVM PLUS on the installation CD-ROM.

2.1.2 CPLD Registers

There are 11 DSP CPLD registers mapped into the DSP's lower CE1 address space starting at address 0x3F0000. Since the CPLD decoder only uses part of the address for decoding, the registers will be mirrored within the space.

The table below shows the bit definitions for the 11 registers in CPLD.

Table 1: CPLD Register Definitions

Addr LSB A4-A1	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
0001	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(Low)	DC_CNTL0 R/W 0(Low)
0010	Reserved								
0011	Reserved								
0100	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
0101	Reserved								
0110	MISC	VCORE_CTL 1	VCORE_CTL 0	Reserved	VCORE_SEL CPLD REGISTERS 0 GPIO 1 BIT 6 & 7 THIS REG	Reserved	TIN0 IN/OUT R/W (0 INPUT)	McBSP2 ON/OFF Board R/W 0 (Onboard)	McBSP0 SROM/ AIC23 Board R/W 0 (SROM)
0111	INT REG	Reserved	Reserved	Reserved	Reserved	WAKEUP INT3	Reserved	WAKUP INT1	WAKEUP INT0
1000	LCD0 Address0	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
1001	LCD1 Address0	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
1010	5502EVM Misc	LCD BUSY R 1 BUSY	LCD_RESET R/W 0	Reserved R	Reserved R	Reserved R	Reserved R	Reserved R	Reserved R

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the 5509A EVM PLUS. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the 5509A EVM PLUS and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	5509A EVM PLUS_VER2	R	Most Significant 5509A EVM PLUS Board Version Bit
1	5509A EVM PLUS_VER1	R	5509A EVM PLUS Board Version Bit
0	5509A EVM PLUS_VER0	R	Least Significant 5509A EVM PLUS Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5509A EVM PLUS, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 bit is used to select whether the DSP's TIN0 (timer) signal is connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

McBSP0SEL and McBSP2SEL control the McBSP0 and McBSP2. Since McBSP0 is used for Serial Boot loading the McBSP.dr pin is routed to the serial ROM at power up. When McBSP0 is used for AIC23B operation this bit must be set to a “1”. McBSP2 is used for MMC operation at power up. Setting this bit to a “1” the McBSP2 is routed to the daughter card connector. The power-on state of these bits (both 0s) represents that situation. Setting the corresponding bit for McBSP2 to “1” enables the McBSP to the expansion daughter-card instead interface.

Table 5: MISC Register

Bit	Name	R/W	Description
7	VCORE_CTL1	R/W	Selects Voltage Control 1
6	VCORE_CTL0	R/W	Selects Voltage Control 0
5	Reserved	R	
4	VCORE_SEL	R/W	0 = GPIO, 1= CPLD Reg bits 6 & 7
3	Reserved	R	
2	TINSEL0	R/W	TIN0 in/out on daughter card (0 = input, 1 = output)
1	MCBSP2SEL	R/W	McBSP2 on/off board (0 = on-board, 1 = off-board)
0	MCBSP0SEL	R/W	McBSP0 on/off board (0 = SROM, 1 = AIC23B)

2.1.7 Interrupt Register

The EVM allows interrupts to be generated from the “Wake Up” switch, S4. These interrupts can be routed to various pins on the VC5509A DSP. The interrupt register does this routing. When the corresponding bit is set to a “1” the DSP will be interrupted by the “Wake Up” switch. The interrupts to choose from are DSP interrupts 0, 1, or 3 as shown in the table below.

Table 6: Interrupt Register

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Wakeup Int3
2	Reserved
1	Wakeup Int1
0	Wakeup Int0

2.1.8 LCD0 Address0 Register

The Liquid Crystal Display (LCD) is a write only interface. It is interfaced via an 8-bit shift register.

Two locations are used when interfacing the LCD panel. Allowing the address bit of the interface to be directly programmed. The shift clock frequency is 3 megahertz.

Writing register LCD0 sets the LCD address line A0 to 0. Writing register LCD1 sets the LCD address line A0 to 1. The write operation to either of these locations starts an internal shift register serializing the data into an 8-bit sequence to the displays.

The table below shows the relationship of the DSP data bits to the LCD data bits.

Table 7: LCD Interface

D7	D6	D5	D4	D3	D2	D1	D0
LCD D7	LCD D6	LCD D5	LCD D4	LCD D3	LCD D2	LCD D1	LCD D0

The figure below shows the LCD data transfer timing. the CPLD automatically generates this timing.

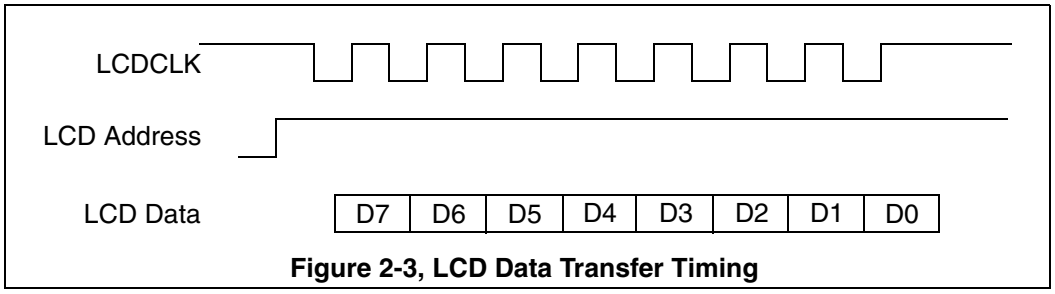


Figure 2-3, LCD Data Transfer Timing

After any write operations the CPLD sets the LCD BUSY bit in the EVM interface Register as the output is being serialized. The user should check this bit prior to starting another write operation. When LCD BUSY is high, the LCD shift register is busy, when is low the shift register is ready.

2.2 AIC23 Codec

The 5509A EVM PLUS uses a Texas Instruments AIC23B (part #TLV320AIC23B) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using I^2C and a McBSPs. The I^2C controls the codec's internal configuration registers. The McBSP is used to send and receive digital audio samples. The control channel is typically only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP0 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The 5509A EVM PLUS examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5509A EVM PLUS.

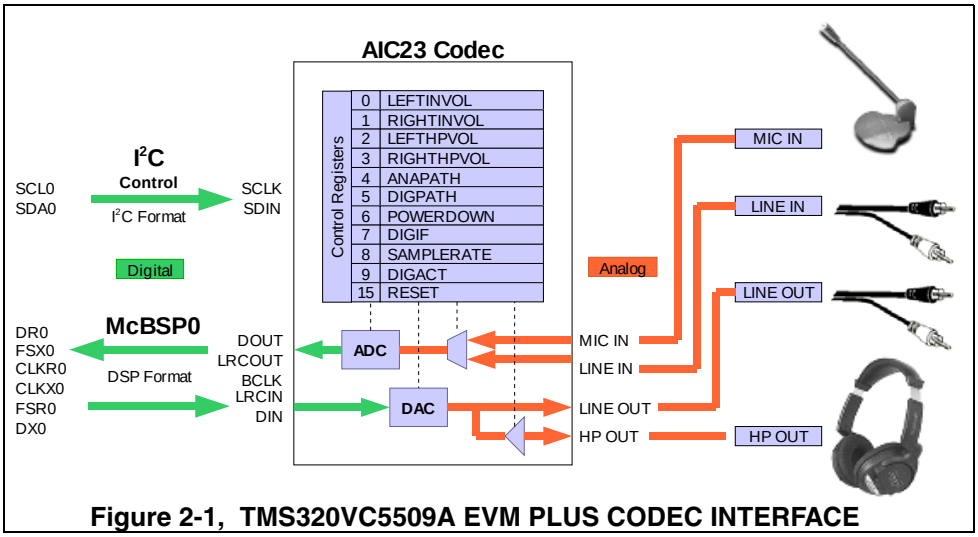


Figure 2-1, TMS320VC5509A EVM PLUS CODEC INTERFACE

2.3 Synchronous DRAM

The 5509A EVM PLUS uses an industry standard 32 megabit Synchronous SDRAM. It uses a 16-bit interface and is used with a 100MHz external memory clock. Since the DSP runs at 200MHz, the EMIF must be programmed to use the SDRAM at half the core clock rate.

The SDRAM occupies both chip enable 0 and 1. It appears on both chip enables because it is twice the size of a single chip enable space. Since the Flash and CPLD use chip enable 1, the 5509A EVM PLUS examples configure CE1 as asynchronous memory for their use and the SDRAM on CE1 is invisible.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

2.4 Flash Memory

The 5509A EVM PLUS provides 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M x 16 parts. The Flash is mapped into CE1 space because that is where the 16-bit asychronous bootloader looks for a boot image when booting from the Flash. The space is shared by the CPLD, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 100ns.

2.5 LEDs and DIP Switches

The 5509A EVM PLUS includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Core Power Control

The C5509A EVM PLUS uses two transistors to modify the feedback to the TPS62000 regulator used to supply the DSP's core voltage. These two transistors form a voltage divider on the feedback to allow the core voltage to switch from 1.6 volts to 1.4 volts to 1.2 volts.

Control of the feedback can be done in 2 ways. The default mechanism is with GPIO5 and GPIO6 of the DSP. The alternative method is to use the 2 bits VCORE_CTL1 and VCORE_CTL0 in the CPLD MISC register. VCORE_SEL in the MISC register determines which mode is used. At power up the register is set to "0" for GPIO mode when VCORE_SEL is set to a "1" the bits 6 and 7 control the voltage control.

2.7 Current Shunts

The C5509A EVM PLUS has 3 shunt devices to convert the small currents of the core, I/O and board currents to voltages. These voltages are then driven into an op-amp which directly interfaces to the National Instruments I/O connector. The shunt resistance, shunt gain, and op-amp gain are shown in the table below.

Table 8: Current Shunts

	Shunt Resistance	Shunt Output Resistance	Op-Amp Gain	Total Gain	Volts per MA	Typical Current	Typical Output
DSP Core	0.1	50K	3	150	.03 volts	150 MA	
DSP I/O	0.1	100K	3	300	.03 volts	5 MA	
EVM	0.025	100K	3	300	.0075 volts	400 MA	

To determine the formula for output voltage to the input current we calculate the value in stages. An example is shown below.

The voltage going into the shunt resistor is derived from:

```
V = IR
```

So for the core current of 1 MA. we have:

```
V = .001 amp  x  .1 ohm = .0001
```

The internal resistance of the shunt current device is 1K ohm. The output is basically a constant current source with a load resistance of 100K(see table above), with this value gain is 100 regardless of the input shunt resistance. So for 1 MA. we have .001 x .1 x 100 at the output of the current shunt amplifier. This is driven into a non-inverting output amplifier with a gain of 3 so we have .001 x .1 x 100 x 3 for .03 volts per milliampere.

2.8 MMC Interface

The VC5509A EVM PLUS supports a multi media card on McBSP2. This port can also be routed to the expansion connector. When bit 1 in register 5 (MISC Reg) is “0” (default) McBSP2 is used for the MMC Interface. When bit 1 register 5 (MISC Reg) is “1” McBSP2 is routed to the expansion daughter connector.

2.9 LCD Display/Keyboard Interface

The C5509A EVM Interface Register implements specific logic for the C5509A EVM. The bits used in this register and their function are described in the table below.

Table 9: C5509A EVM PLUS Interface

Bit	Name	R/W	Description
7	LCD Busy	R	0 = busy, not ready, 1 = not busy, ready
6	LCD Reset	R/W	0 = removes reset from LCD, 1 = forces LCD into reset
5	Reserved	R	
4	Reserved	R	
3	Reserved	R	
2	Reserved	R	
1	Reserved	R	
0	Reserved	R	

LCD Busy indicates the status of the CPLD implemented shift register which interfaces to the LCD panel. A 1 logic level indicates the shift register is busy, A 0 logic level indicates the shift register is ready.

LCD Reset allows the LCD Reset bit to be toggled under software control. A 1 logic level forces the LCD panel into reset. A 0 logic level removes the LCD reset to normal state.

2.10 Daughter Card Interface

The 5509A EVM PLUS provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their 5509A EVM PLUS platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory and peripherals.

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the 5509A EVM PLUS board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The 5509A EVM PLUS also multiplexes the McBSP2 for on-board or external use.
This function is controlled through the CPLD MISC register.

The timer signals on the peripheral expansion connector have connections for both inputs and outputs. since the VC5509A does not have separate timer inputs and outputs, the CPLD is used to select whether the input or output pin should be connected to the timer. This selection is also controlled through the CPLD MISC register.

Chapter 3

Physical Description

This chapter describes the physical layout of the TMS320VC5509A EVM PLUS and its connectors.

Topic **Page**

3.1 Board Layout

The VC5509A EVM PLUS is a 8.25 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the VC5509A EVM PLUS.

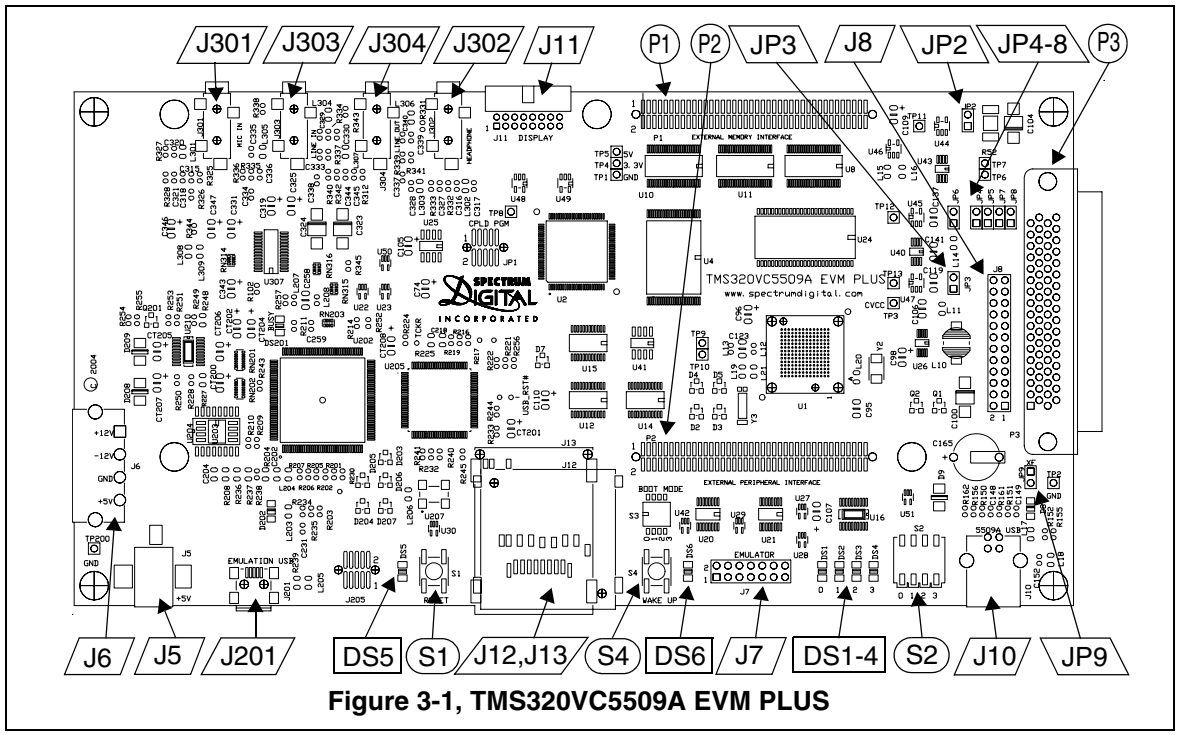


Figure 3-1, TMS320VC5509A EVM PLUS

3.2 Connector Index

The TMS320VC5509A EVM PLUS has many connectors which provide the user access to the various signals on the DSK.

Table 1: TMS320VC5509A EVM PLUS Connectors

Connector	# Pins	Function
P1	80	Memory
P2	80	Peripheral
P3	68	National Instruments Interface
J301	2	Microphone
J303	2	Line In
J304	2	Line Out
J302	2	Headphone
J5	2	+5 Volt
J6 *	4	Optional Power Connector
J7	14	External JTAG
J8	24	National Instruments Prototype Header
J11	16	Keypad/Display Interface
J12		MultiMedia Card
J201	5	USB Port
JP1	10	CPLD Programming

Note: "*" Not populated

3.3 Expansion Connectors

The TMS320VC5509A EVM PLUS supports two expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following two sections.

The two expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: I is on an Input pin
O is on an Output pin
Z is on a High Impedance pin

3.3.1 P1, Memory Expansion Connector

Table 2: P1, Memory Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+5 Volts	O	2	+5 volts	O
3	A20	O	4	A19	O
5	A18	O	6	A17	O
7	A16	O	8	A15	O
9	A14	O	10	A13	O
11	GND	O	12	GND	O
13	A12	O	14	A11	O
15	A10	O	16	A9	O
17	A8	O	18	A7	O
19	A6	O	20	A5	O
21	+5 Volts	O	22	+5 Volts	O
23	A4	O	24	A3	O
25	A2	O	26	A1	O
27	Reserved		28	Reserved	
29	BE1n	O	30	BE0n	O
31	GND	O	32	GND	O
33	Reserved		34	Reserved	
35	Reserved		36	Reserved	
37	Reserved		38	Reserved	
39	Reserved		40	Reserved	
41	+3.3 Volts	O	42	+3.3 Volts	O
43	Reserved		44	Reserved	
45	Reserved		46	Reserved	
47	Reserved		48	Reserved	
49	Reserved		50	Reserved	
51	GND	O	52	GND	O
53	D15	I/O/Z	54	D14	I/O/Z
55	D13	I/O/Z	56	D12	I/O/Z
57	D11	I/O/Z	58	D10	I/O/Z
59	D9	I/O/Z	60	D8	I/O/Z
61	GND	O	62	GND	O
63	D7	I/O/Z	64	D6	I/O/Z
65	D5	I/O/Z	66	D4	I/O/Z
67	D3	I/O/Z	68	D2	I/O/Z
69	D1	O	70	D0	O
71	GND	O	72	GND	O
73	REn	O	74	WEn	O
75	OEn	O	76	RDYn	I
77	CE3n	O	78	CE2n	O
79	GND	O	80	GND	O

3.3.2 P2, Peripheral Expansion Connector

Table 3: P2, Peripheral Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+12 Volts *	O	2	-12 Volts *	O
3	GND	O	4	GND	O
5	+5 Volts	O	6	+5 Volts	O
7	GND	O	8	GND	O
9	+5 Volts	O	10	+5 Volts	O
11	RESERVED		12	RESERVED	
13	RESERVED		14	RESERVED	
15	RESERVED		16	RESERVED	
17	RESERVED		18	RESERVED	
19	+3.3 Volts	O	20	+3.3 Volts	O
21	CLKX1	I/O/Z	22	RESERVED	
23	FSX1	I/O/Z	24	DX1	O/Z
25	GND	O	26	GND	O
27	CLKR1	I/O/Z	28	RESERVED	
29	FSR1	I/O/Z	30	DR1	I
31	GND	O	32	GND	O
33	CLKX2	I/O/Z	34		
35	FSX2	I/O/Z	36	DX2	O/Z
37	GND	O	38	GND	O
39	CLKR2	I/O/Z	40	RESERVED	
41	FSR2	I/O/Z	42	DR2	Z
43	GND	O	44	GND	O
45	TOUT0	Z	46	TIN0	I
47	INT0n	I	48	INT2n	I
49			50		
51	GND	O	52	GND	O
53	INT1n	I	54		
55	RESERVED		56		
57	RESERVED		58	INT4n	I
59	RESETn	O	60	RESERVED	
61	GND	O	62	GND	O
63	DC_CNTL1	O	64	DC_CNTL0	O
65	DC_STAT1	I	66	DC_STAT0	I
67	INT3n	I	68	RESERVED	
69	RESERVED		70	RESERVED	
71	RESERVED		72	RESERVED	
73	RESERVED		74	RESERVED	
75	DETECTn	I	76	GND	O
77	GND	O	78	CLKOUT	O
79	GND	O	80	GND	O

3.3.3 P3, National Instruments Interface

The VC5509A EVM PLUS provides a direct connection to the National Instruments series of instrumentation products.

Only a limited selection of the available inputs and outputs are used by the EVM at this time. Some of the spare signals are routed to the test headers for prototyping use.

Note that it is important to realize that the voltages for the National Instruments products and the EVM products often require level translation. Do not connect signals to this interface prior to familiarizing yourself with these requirements. The table below shows the signals on this interface.

Table 4: P3, National Instruments Interface

Pin #	Signal Name	I/O/Z	EVM Function	Pin #	Signal Name	I/O/Z	EVM Function
1	FREQ_OUT			35	DGND		
2	GPCTR0_OUT			36	DGND		
3	PFI9/GPCTR0_GATE			37	PFI8/GPCTR0_SOURCE		
4	DGND			38	PFI7/STARTSCAN		
5	PFI6/WFTRIG			39	DGND		
6	PFI5/UPDATE			40	GPCTR1_OUT		
7	DGND			41	PFI4/GPCTR1_GATE		
8	+5 v			42	PFI3/GPCTR1_SOURCE		
9	DGND			43	PFI2/CONVERT		
10	PFI1/TRIG2			44	DGND		
11	PFI0/TRIG1			45	EXTSTROBE		
12	DGND			46	SCANCLK		
13	DGND			47	DIO3		
14	+5 V			48	DIO7		
15	DGND			49	DIO2		
16	DIO6			50	DGND		
17	DIO1			51	DIO5		
18	DGND			52	DIO0		
19	DIO4			53	DGND		
20	EXTREF			54	AOGND		
21	DAC1OUT			55	AOGND		
22	DAC0OUT			56	AIGND		
23	ACH15			57	ACH7		
24	AIGND			58	ACH14		
25	ACH6			59	AIGND		
26	ACH13			60	ACH5		
27	AIGND			61	ACH12		
28	ACH4			62	AISENSE		
29	AIGND			63	ACH11		
30	ACH3			64	AIGND		
31	ACH10			65	ACH2		
32	AIGND			66	ACH9		
33	ACH1			67	AIGND		
34	ACG8			68	ACH0		

3.3.3.1 Analog Probe Connectors

Four connectors are available from the National Instruments connector for analog probing. The two inputs and two outputs are shown in the table below.
The signal names on each pin are shown in the table below.

Table 5: Analog Probe Connectors

Connector	Signal Name
JP4, Pin 1	P3 Analog Out 0
JP4, Pin 2	Ground
JP5, Pin 1	P3 Analog Out 1
JP5, Pin 2	Ground
JP6, Pin 1	P3 Analog In 6
JP6, Pin 2	Ground
JP7, Pin 1	P3 Analog In 7
JP7, Pin 2	Ground

3.3.3.2 National Instruments Prototype Header

The National Instruments Prototype Header is 2 x 12 double row header. This allows users to prototype signals to be feedback into the National Instruments interface.
The signal names on each pin are shown in the table below.

Table 6: National Instruments Prototype Header

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	P3 Pin 1		2	P3 Pin 2	
3	P3 Pin 37		4	P3 Pin 3	
5	P3 Pin 38		6	P3 Pin 5	
7	P3 Pin 40		8	P3 Pin 6	
9	P3 Pin 42		10	P3 Pin 41	
11	P3 Pin 10		12	P3 Pin 43	
13	P3 Pin 45		14	P3 Pin 11	
15	P3 Pin 47		16	P3 Pin 46	
17	P3 Pin 49		18	P3 Pin 48	
19	P3 Pin 51		20	P3 Pin 16	
21	P3 Pin 60		22	P3 Pin 19	
23	P3 Pin 28		24	**P3 Pin _____**	

3.3.4 J11, Keypad/Display Interface

Connector J11 is a 16 pin interface to the Spectrum Digital keypad/display module. The signals on this connector are shown in the table below.

Table 7: J11, Keypad/Display Interface

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+3.3 volts		2	+3.3 Volts	
3	Analog In 0		4	Analog In 1	
5	LCD_Data		6	LCD_Address	
7	LCD_Reset		8	LCD_CLK	
9	Ground		10	Ground	
11	I^2C Data		12	Ground	
13	I^2C CLK		14	Ground	
15	+3.3 Volts		16	+3.3 Volts	

The display is interfaced via the CPLD in an SPI type format. The switches and potentiometers are connected to I^2C analog to digital converters and also supplied as analog voltages to the VC5509A's analog inputs.

For more information on the display please reference the Universal Display Technical Reference Manual.

3.3.5 J12, SD/MMC Interface

Connector J12 is a 12 pin interface to MMC module. The signals on this connector are shown in the table below.

Table 8: J12, SD/MMC Interface

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	MMC.DAT3		2	MMC.CMD	
3	Ground		4	+3.3 Volts	
5	MMC.CLK		6	Ground	
7	MMC.DAT0		8	MMC.DAT1	
9	MMC.DAT2		10	Write protect - N/C	
11	Ground		12	Media Present - N/C	

3.4 Audio Connectors

The VC5509A EVM PLUS has 4 audio connectors. They are described in the following sections.

3.4.1 J301, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

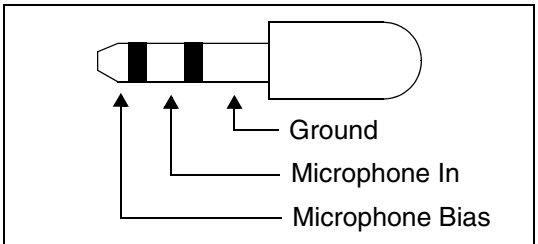


Figure 3-2, Microphone Stereo Jack

3.4.2 J303, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

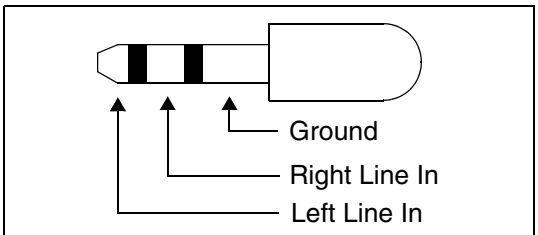


Figure 3-3, Audio Line In Stereo Jack

3.4.3 J304, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

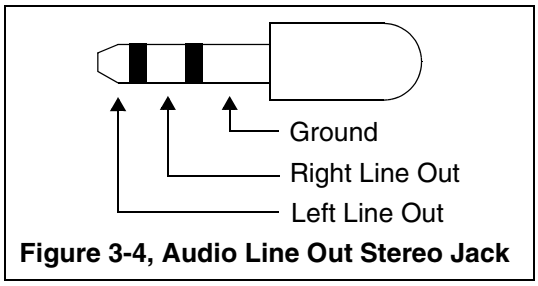


Figure 3-4, Audio Line Out Stereo Jack

3.4.4 J302, Headphone Connector

Connector J4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below

.

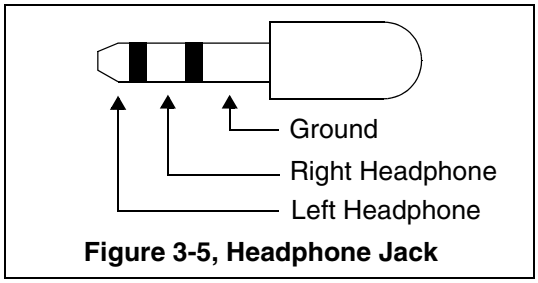


Figure 3-5, Headphone Jack

3.5 Power Connectors

The VC5509A EVM PLUS has 2 power connectors. They are described in the following sections.

3.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320VC5509A EVM PLUS via the J5 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.

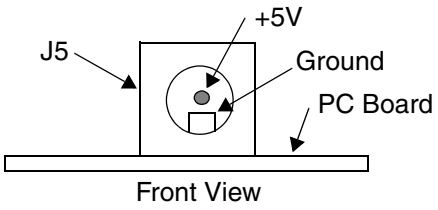


Figure 3-6, TMS320VC5509A EVM PLUS Power Connector

3.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15109-0410 or Tyco #174552-1. The table below shows the voltages on the respective pins.

Table 9: J6, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

3.6 Miscellaneous Connectors

The VC5509A EVM PLUS has 3 additional connectors to aid the user in developing with this product. They are described in the following sections.

3.6.1 J201, Mini USB Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

Table 10: J201, USB Connector

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

3.6.2 J7, External JTAG Connector

The TMS320VC5509A EVM PLUS is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

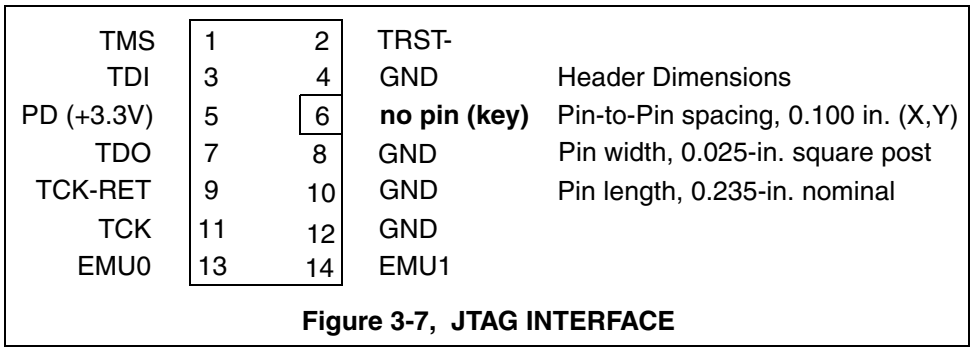


Figure 3-7, JTAG INTERFACE

3.6.3 JP1, PLD Programming Connector

This connector interfaces to the Altera CPLD, U2. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

3.7 User LEDs

The VC5509A EVM PLUS provides 4 LEDs which show selftest status at power up and are available for application programs or demonstrations. The LEDs are accessed via the user register of the CPLD. For more information on the control of the LEDs refer to the user register section of the CPLD.

3.8 System LEDs

TheTMS320VC5509A EVM PLUS has three system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

Table 11: System LEDs

Reference Designator	Color	Function	On Signal State
DS6	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.	1
DS5	Orange	RESET Active	1
DS201	Green	USB Active, Blinks during USB data transfer	1

3.9 User DIP Switch

S2 is a 4 position DIP switch to be used by application and demonstration programs. The switch is mapped into the CPLD and can be accessed via the User register. For more details see the section on CPLD register 2, User register.

3.10 Reset Switch

There are three resets on the TMS320VC5509A EVM PLUS. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5509A.

External sources which control the reset are push button S1, and the on board embedded USB JTAG emulator.

3.11 Wake Up Switch

S4 is a “Wake Up” switch to the DSP. When the DSP is in idle mode the switch can generate an interrupt to wake up the DSP. See the section on the CPLD Interrupt register to enable interrupts for the “Wake Up” switch

3.10 Test Points

The VC5509A EVM PLUS has thirteen (13) test points. Their position is shown in the diagram below.

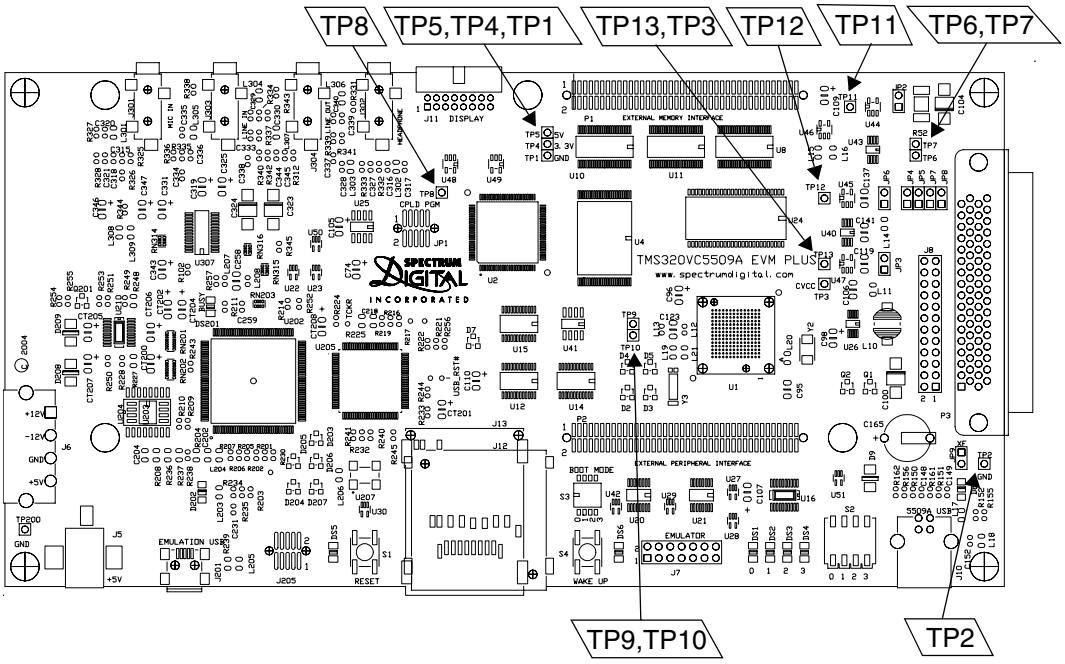


Figure 3-x, TMS320VC5509A EVM PLUS Test Points

The table below shows the signals present on each test point.

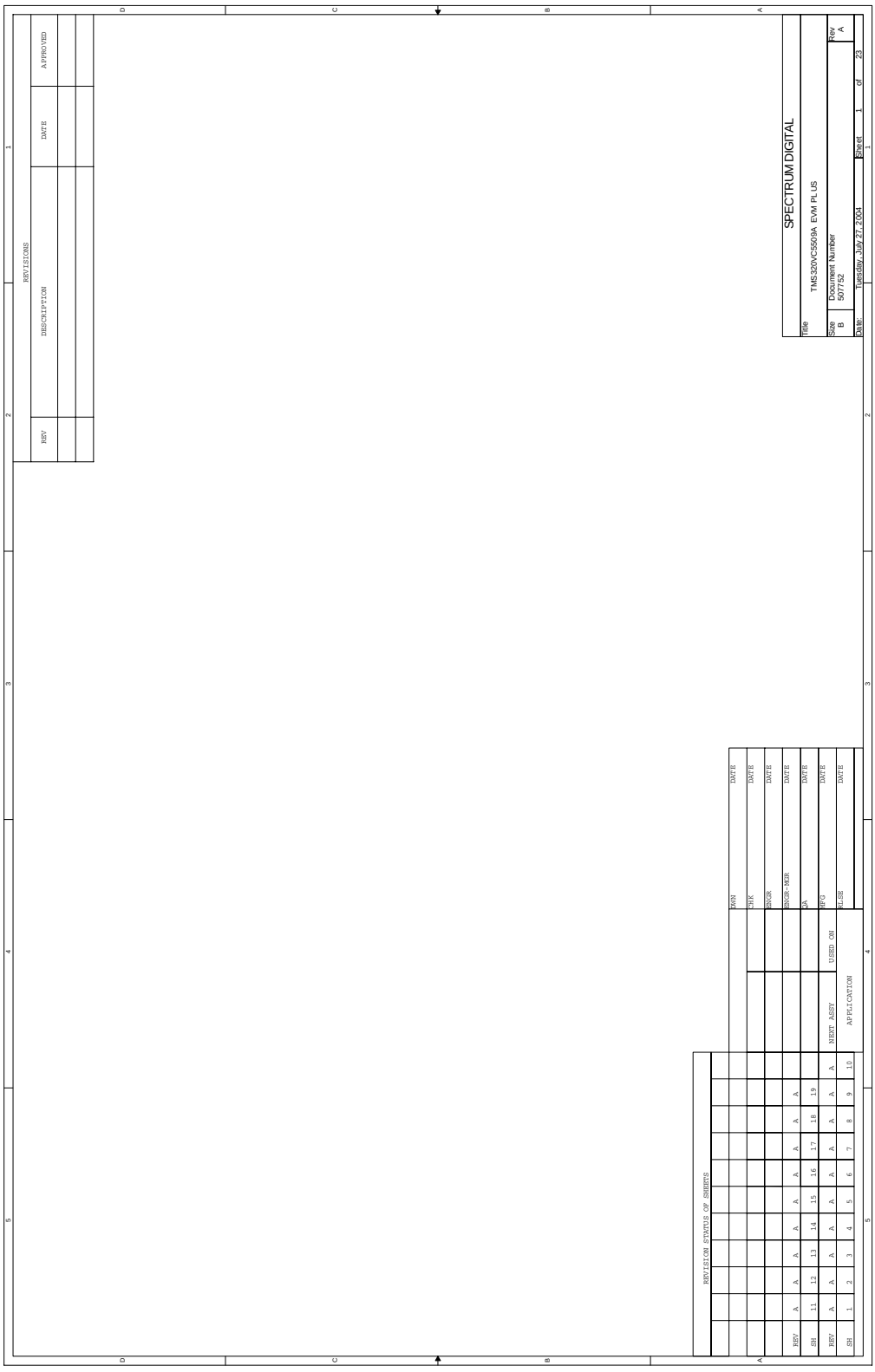
Table 12: TMS320VC5509A EVM Plus Test Points

Test Point #	Signal
TP1	Ground
TP2	Ground
TP3	DSP Core Voltage
TP4	+3.3 Volts
TP5	+5 Volts
TP6	DIGIO0
TP7	DIGIO1
TP8	CPLD Spare
TP9	Ground
TP10	
TP11	+5 Volt Current Shunt Output
TP12	+3.3 Volt Current Shunt Output
TP13	DSP Core Current Shunt Output

Appendix A

Schematics

This appendix contains the schematics for the TMS320VC5509A EVM PLUS. Board components with designators over 200 (e.g. DS210, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.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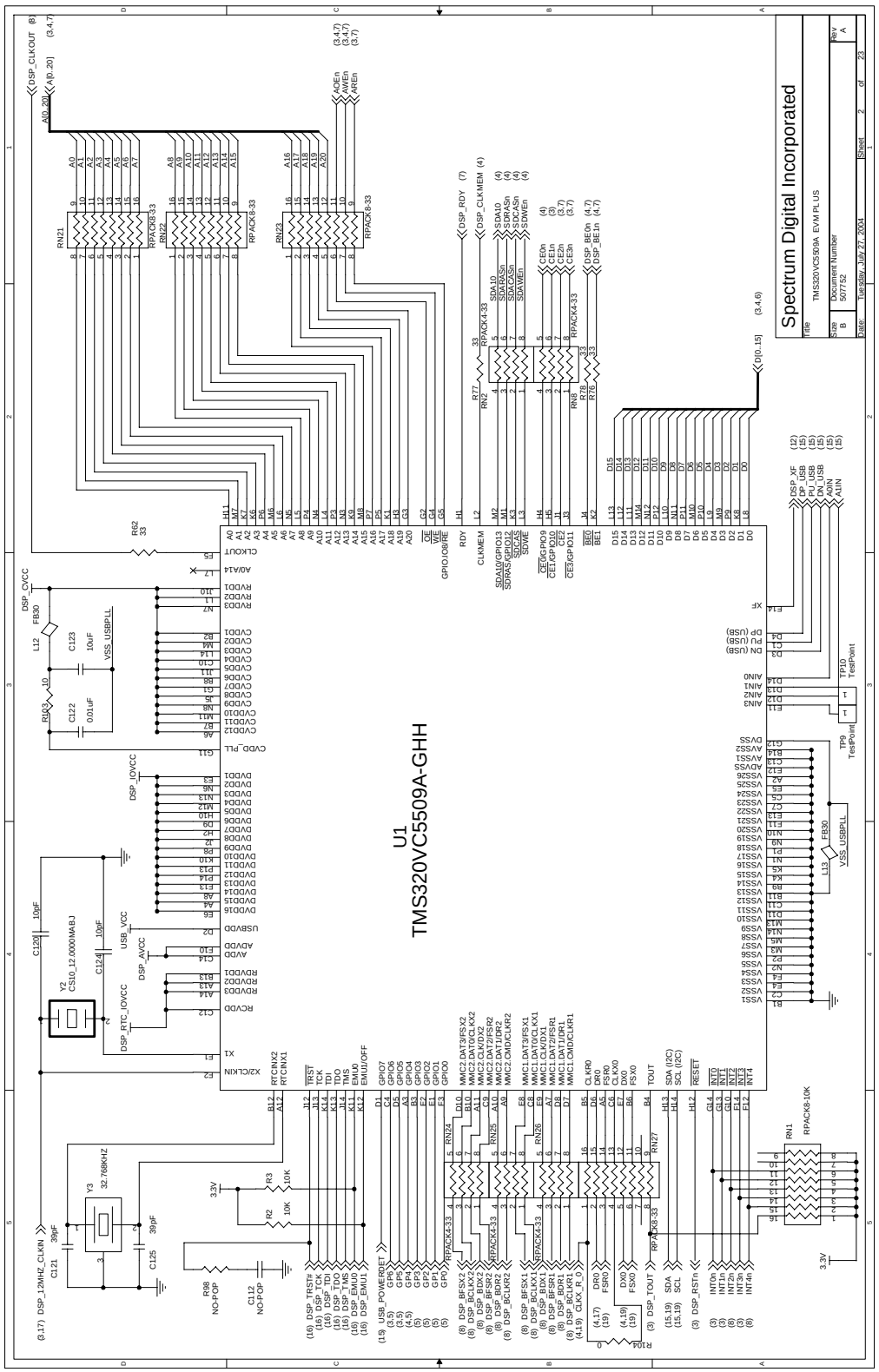
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TMS320VC5509A EVM PLUS
Document Number
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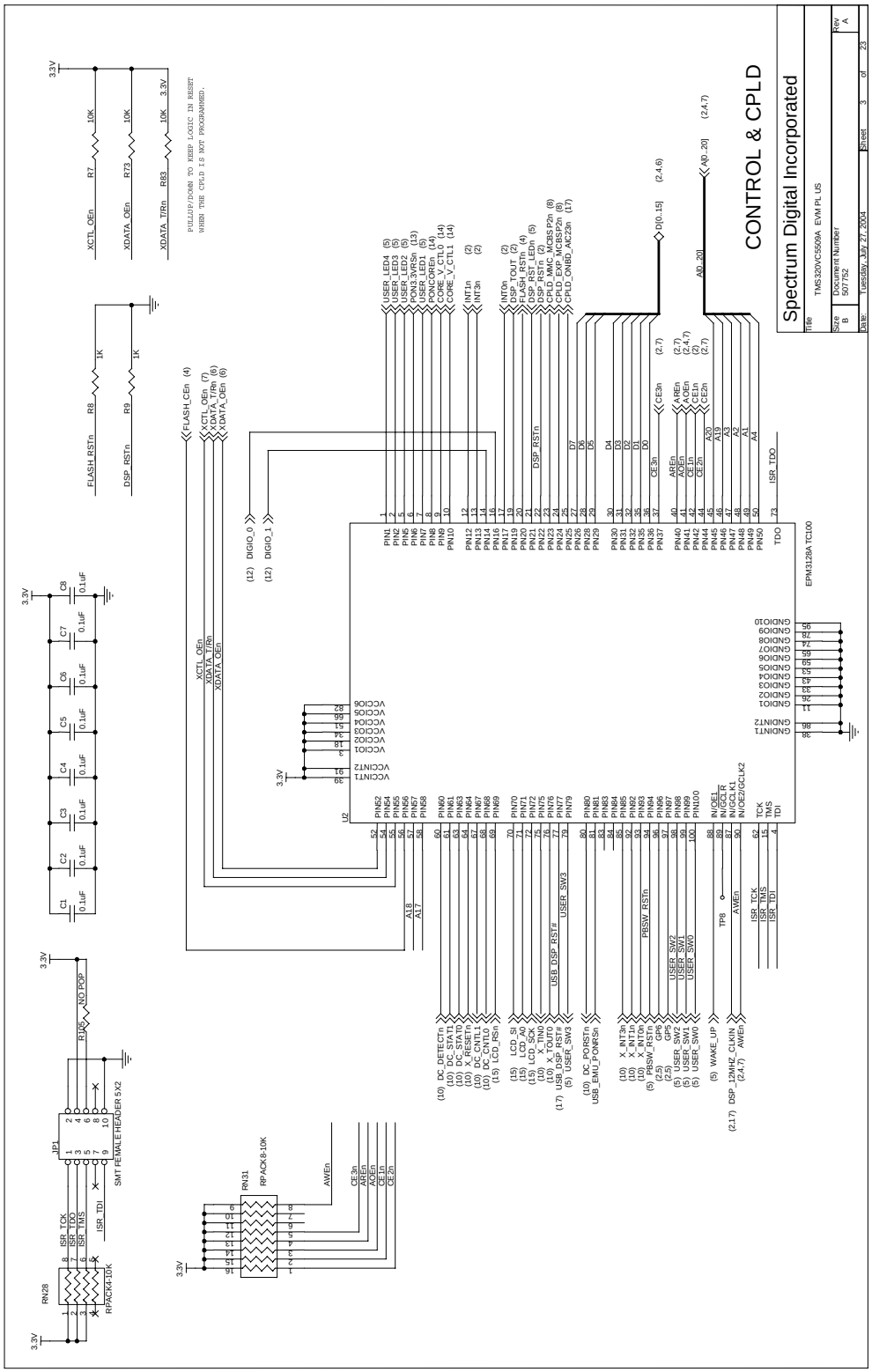
CONTROL & CPLD
Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
EPM3128A TC100
U2
JP1
SMT FEMALE HEADER 5X2
RN28
RN31
RPACK8-10K
RPACK4-10K
RJ45_ADD POP
FLASH_CEn
XCTL_OEn
XDATA_T/Rn
XDATA_OEn
DSP_RSTn
FLASH_RSTn
R7
R73
R83
R8
R9
10K
1K
C1
C2
C3
C4
C5
C6
C7
C8
0.1uF
3.3V
USER_LED4
USER_LED3
USER_LED2
PON3.3VRSn
USER_LED1
PON2.5VRSn
CORE_V_CTL0
CORE_V_CTL1
INT1n
INT3n
INT0n
DSP_TOUT
FLASH_RSTn
DSP_RST_LEDn
DSP_RSTn
CPLD_MMC_MCBSP2n
CPLD_EXP_MCBSP2n
CPLD_ONBD_AIC23n
D[0..15]
A[0..20]
CE3n
AREn
AOEn
CE1n
CE2n
ISR_TDO
DIGIO_0
DIGIO_1
DC_DETECTn
DC_STAT1
DC_STAT0
DC_RESETn
DC_CNTL1
DC_CNTL0
LCD_RSn
LCD_SI
LCD_A0
LCD_SCK
LCD_CSn
X_TOUT0
USB_DSP_RST#
USER_SW3
DC_PORSTn
USB_EMU_PONRSn
X_INT3n
X_INT1n
X_INT0n
PBSW_RSTn
GPIO6
GPIO5
USER_SW2
USER_SW1
USER_SW0
WAKE_UP
AWEn
DSP_12MHZ_CLKIN
ISR_TCK
ISR_TMS
ISR_TDI
TCK
TMS
TDI
TDO
GNDIO10
GNDIO9
GNDIO8
GNDIO7
GNDIO6
GNDIO5
GNDIO4
GNDIO3
GNDIO2
GNDIO1
GNDINT2
GNDINT1
VCCIO8
VCCIO5
VCCIO4
VCCIO3
VCCIO2
VCCIO1
VCCINT2
VCCINT1
PULLUP/DOWN TO KEEP LOGIC IN RESET
WHEN THE CPLD IS NOT PROGRAMMED.
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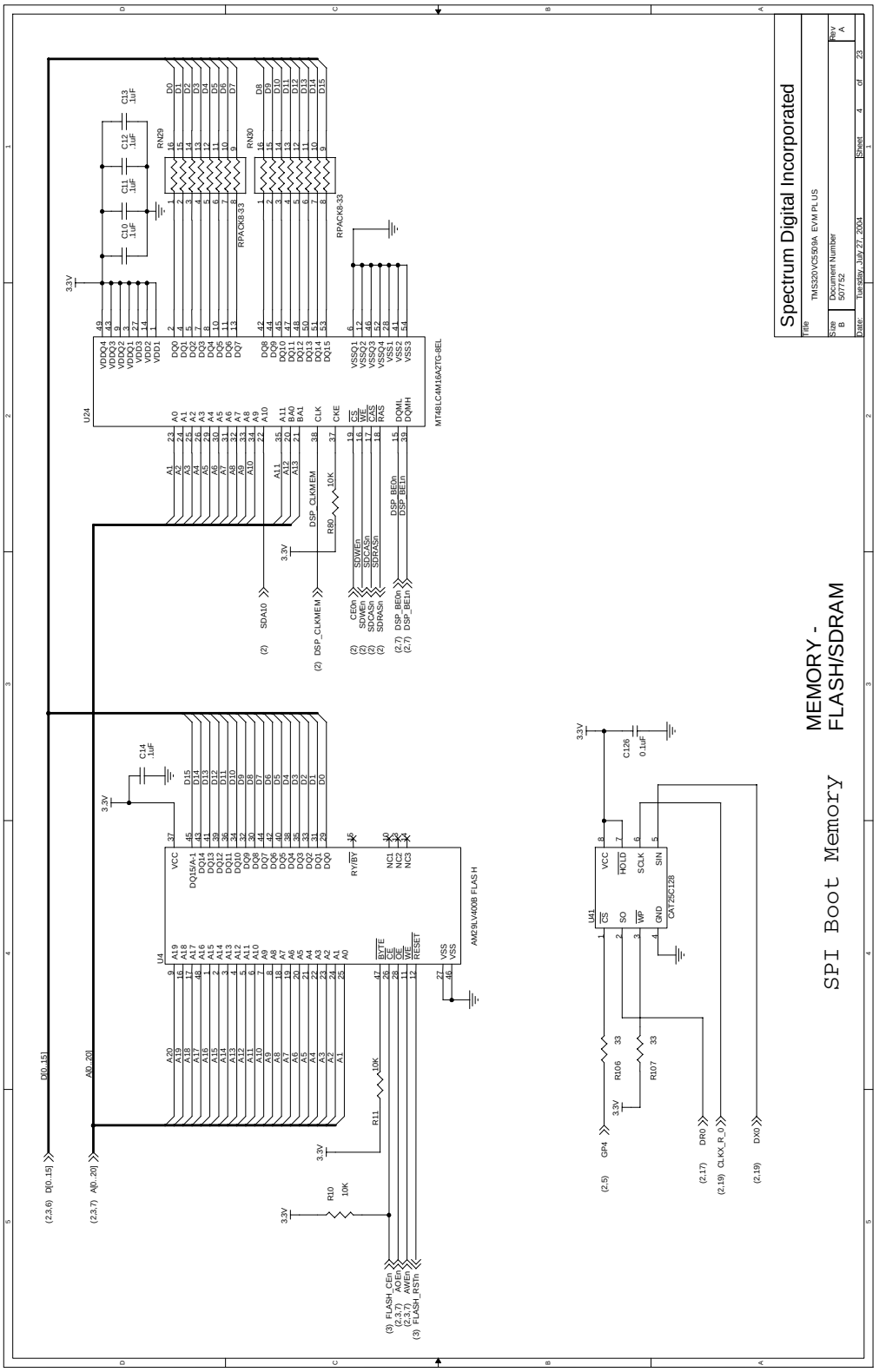
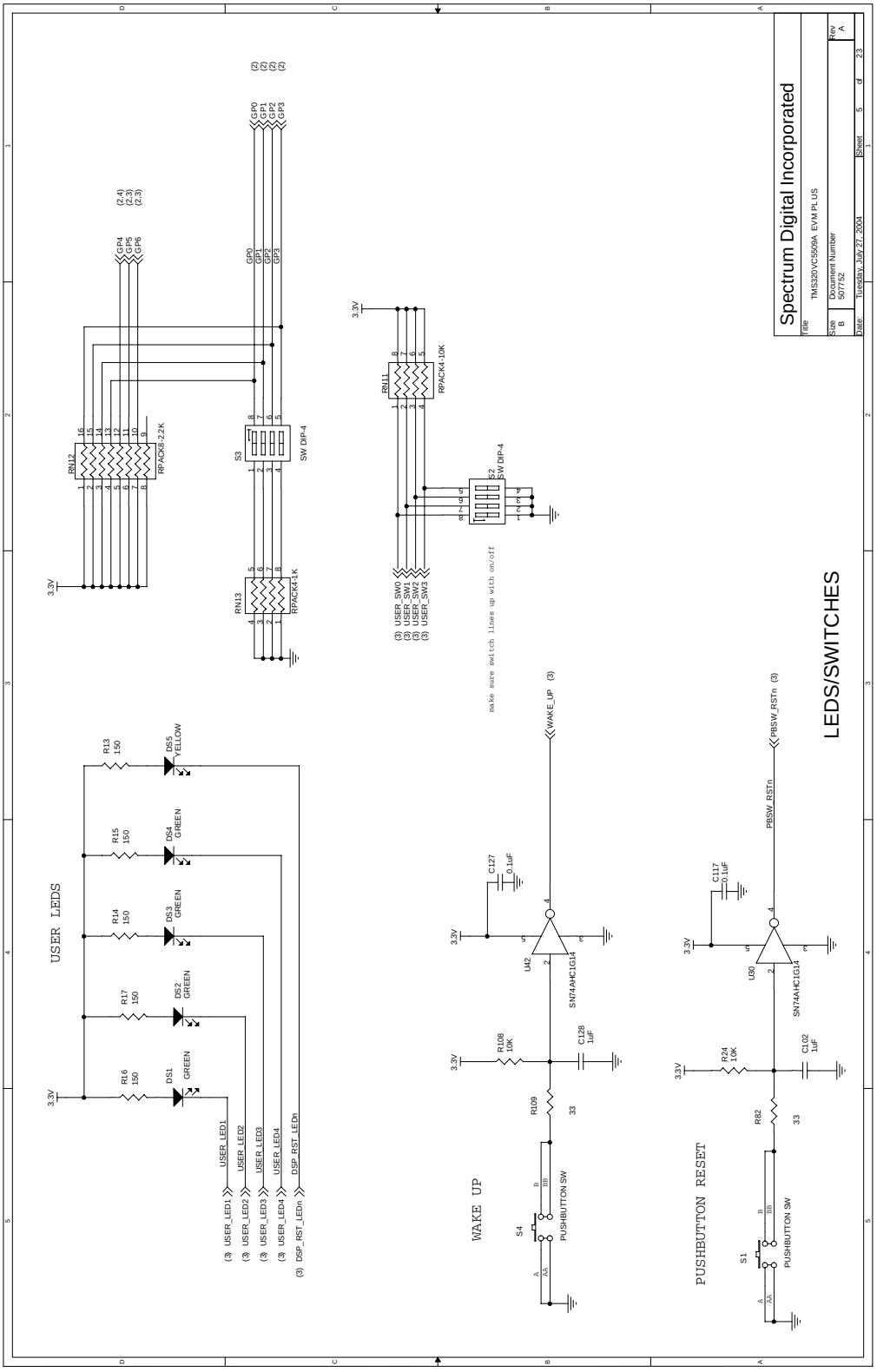
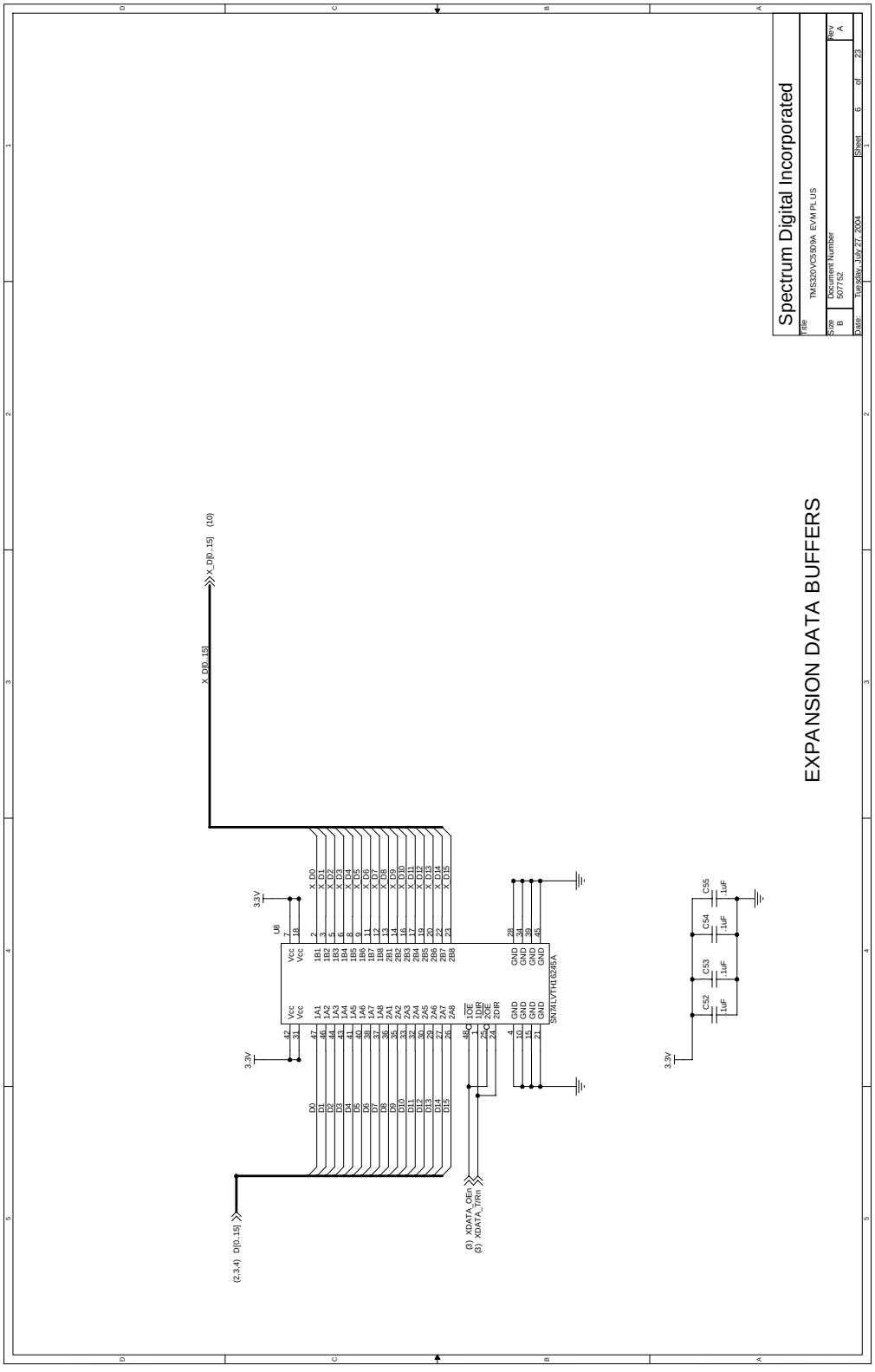

Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
MEMORY - FLASH/SDRAM
SPI Boot Memory
U24
MT48LC4M16A2TG-8EL
U4
AM29LV400B FLASH
U41
CAT25C128
RPACK8-33
RN29
RN30
R10
R11
R80
R106
R107
C10 .1uF
C11 .1uF
C12 .1uF
C13 .1uF
C14 .1uF
C126 0.1uF
3.3V
D[0..15]
A[0..20]
SDA10
DSP_CLKMEM
CEDn
SDWEn
SDCASn
SDRASn
DSP_BEDn
DSP_BEIn
FLASH_CEn
AOEn
AWEn
FLASH_RSTn
GP4
DR0
CLKX_R_0
DX0


Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
LEDS/SWITCHES
USER LEDS
WAKE UP
PUSHBUTTON RESET
make sure switch lines up with on/off
PUSHBUTTON SW
SW DIP-4
RPACK8-2.2K
RPACK4-10K
RPACK4-1K
SN74AHC1G14
3.3V
USER_LED1
USER_LED2
USER_LED3
USER_LED4
DSP_RST_LEDn
WAKE_UP
PBSW_RSTn
USER_SW0
USER_SW1
USER_SW2
USER_SW3


Spectrum Digital Incorporated
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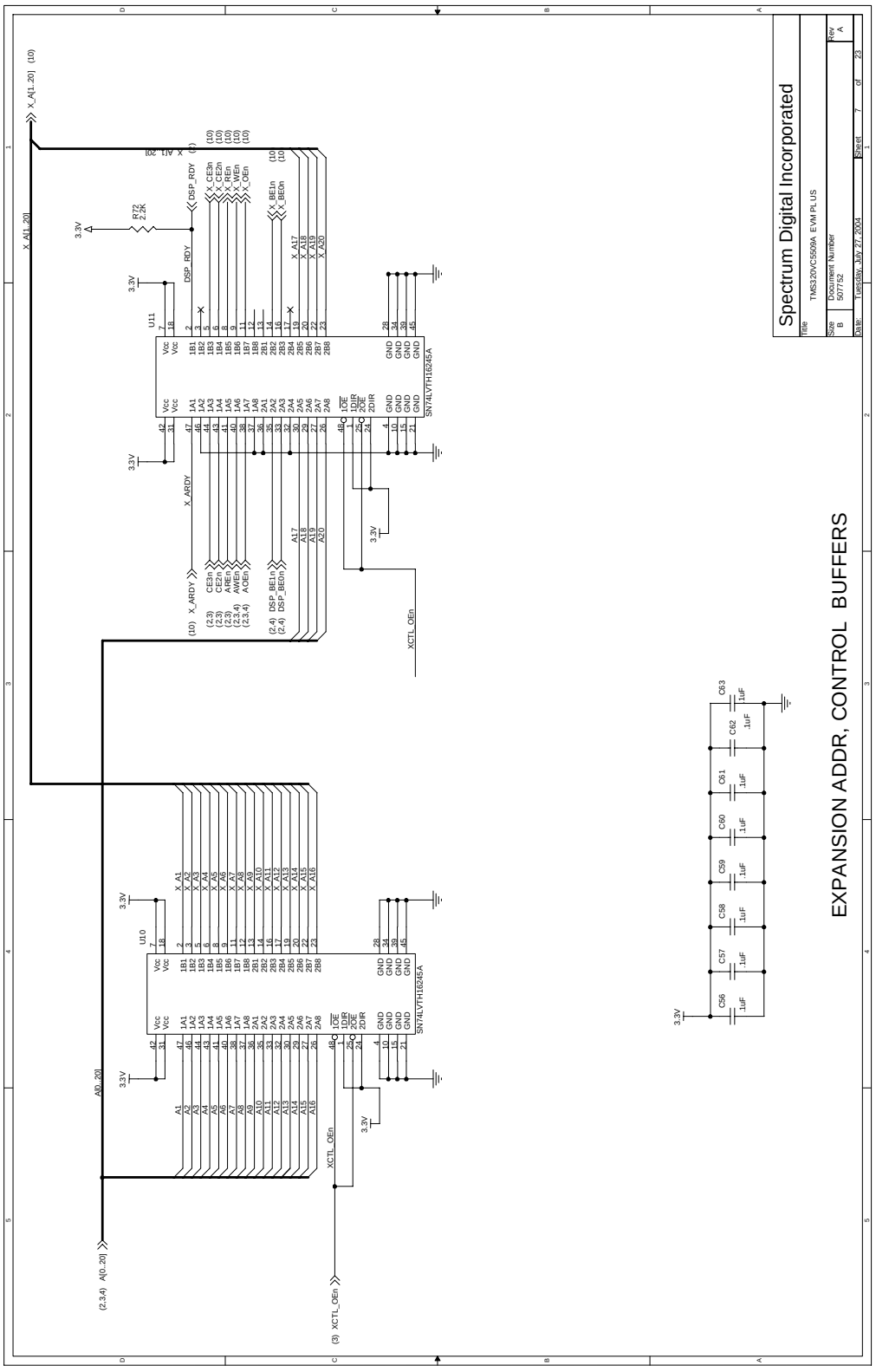
23
EXPANSION DATA BUFFERS
X_D[0..15]
D[0..15]
(2,3,4)
(3) XDATA_OEn
(3) XDATA_TrRn
U8
SN74LVTH16245A
3.3V
C52
C53
C54
C55
1uF


Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
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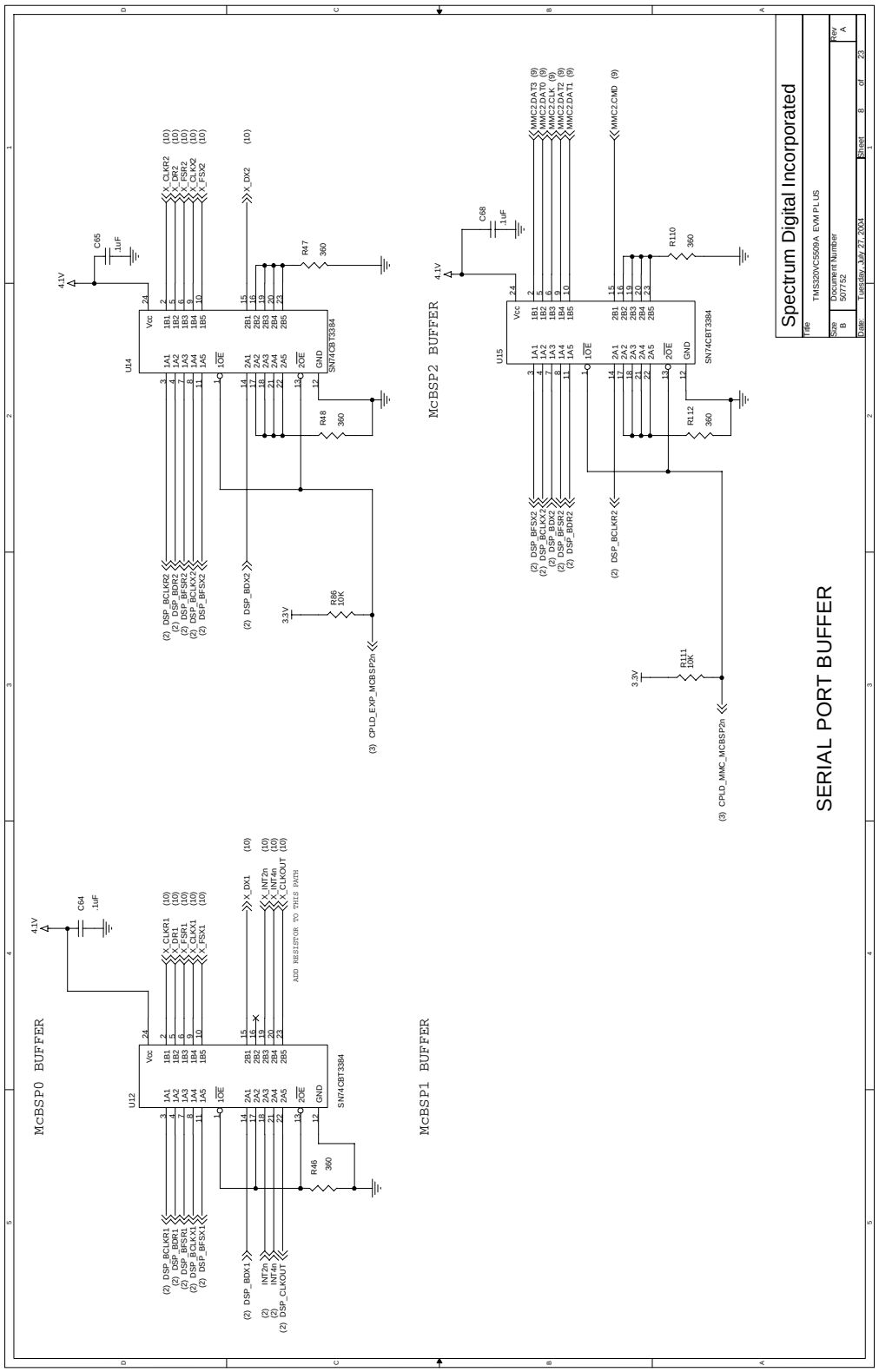
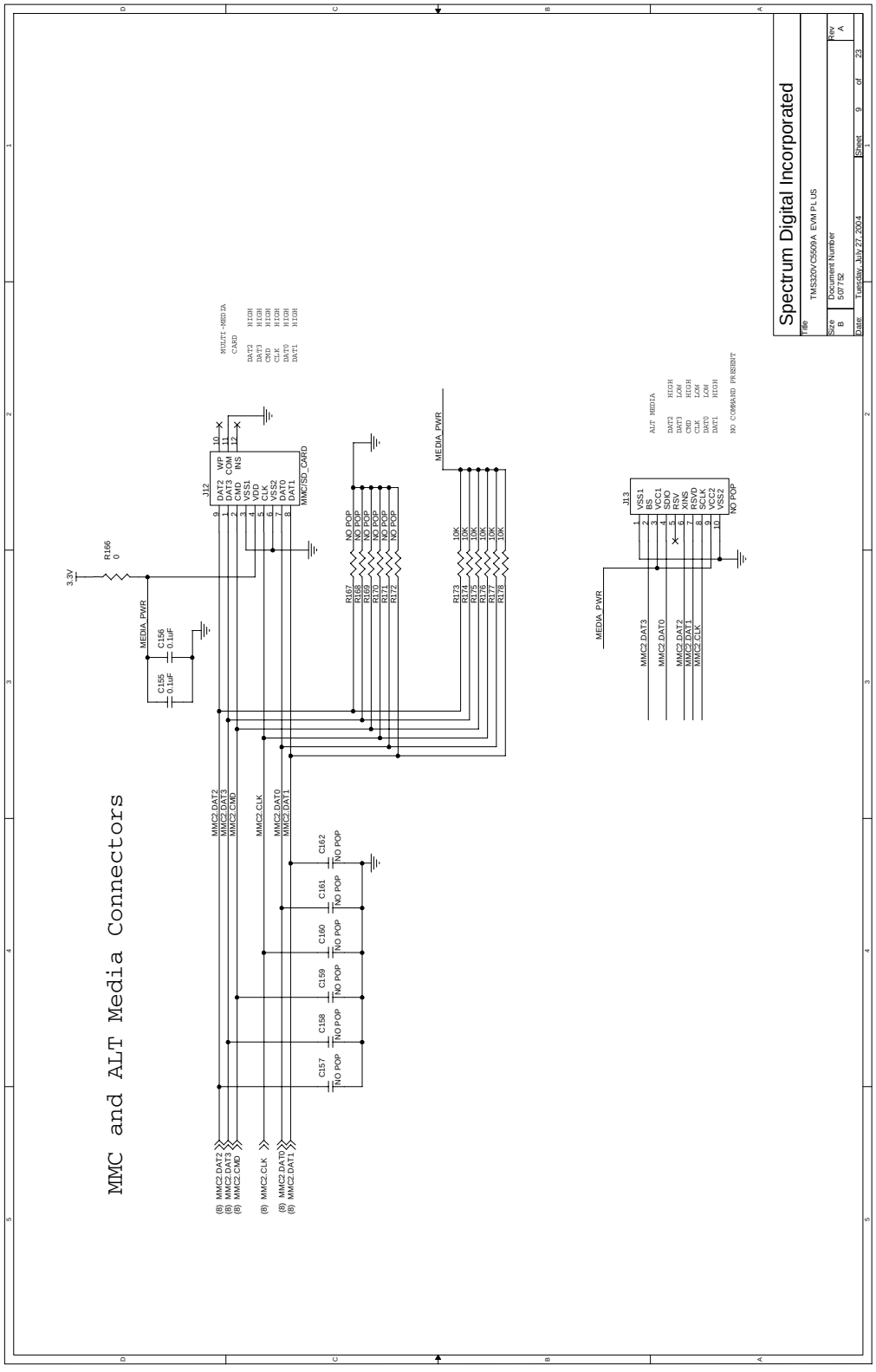
EXPANSION ADDR, CONTROL BUFFERS
SN74LVTH16245A
X_A[1..20]
A[0..20]
X_ARDY
DSP_RDY
XCTL_OEn
X_CE3n
X_CE2n
X_CE1n
X_WEn
X_OEn
X_BE1n
X_BE0n
3.3V


SERIAL PORT BUFFER
McBSP0 BUFFER
McBSP1 BUFFER
McBSP2 BUFFER
Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
SN74CBT3384
ADD RESISTOR TO THIS PATH


MMC and ALT Media Connectors
Spectrum Digital Incorporated
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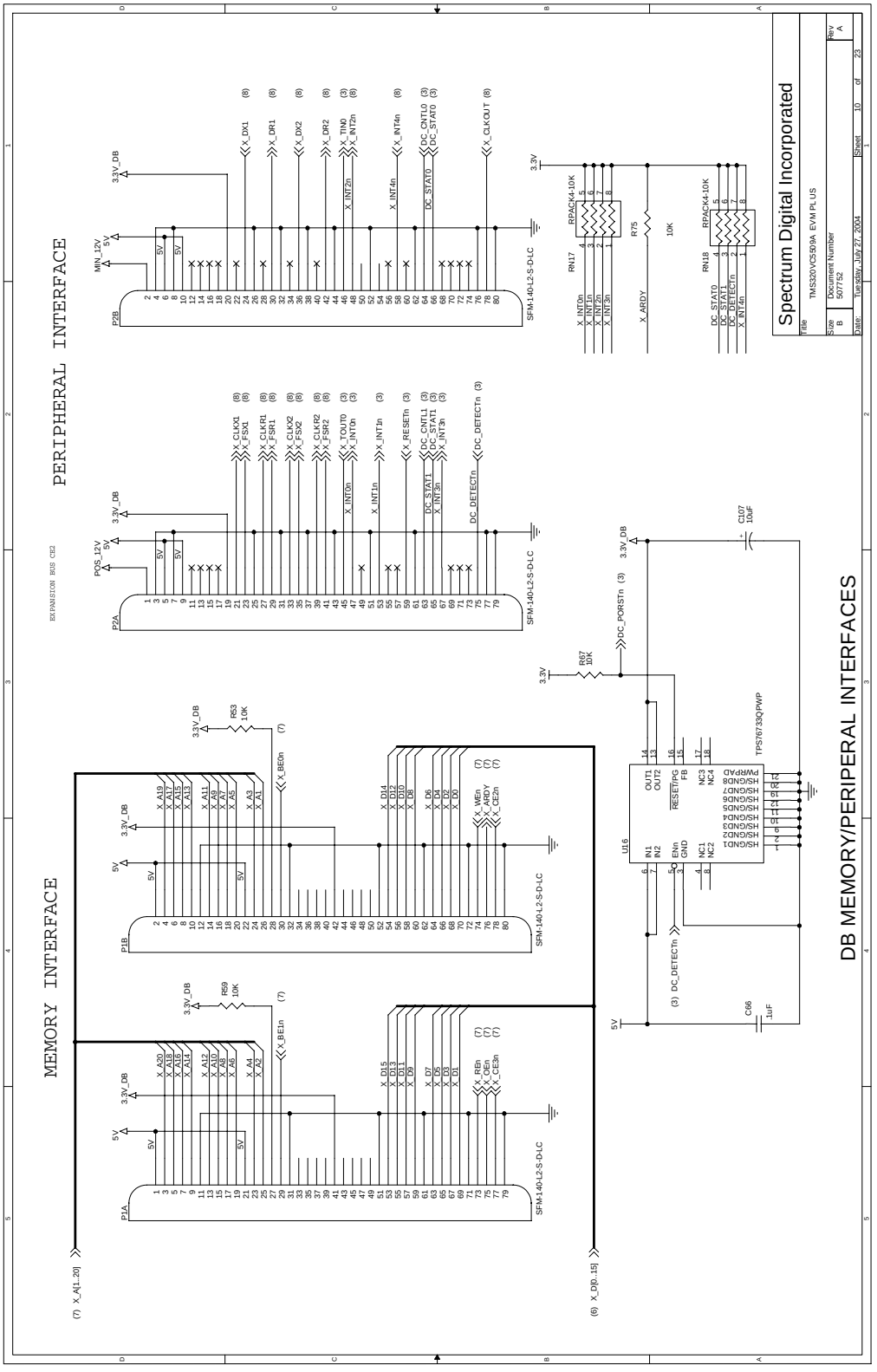
MEDIA_PWR
3.3V
R166 0
C155 0.1uF
C156 0.1uF
J12
MMC/SD_CARD
MULTI-MEDIA CARD
DAT2 HIGH
DAT3 HIGH
CMD HIGH
CLK HIGH
DAT0 HIGH
DAT1 HIGH
R167 NO POP
R168 NO POP
R169 NO POP
R170 NO POP
R171 NO POP
R172 NO POP
R173 10K
R174 10K
R175 10K
R176 10K
R177 10K
R178 10K
J13
ALT MEDIA
DAT2 HIGH
DAT3 HIGH
CMD HIGH
CLK LOW
DAT0 LOW
DAT1 HIGH
NO COMMAND PRESENT
NO POP
MMC2_DAT2
MMC2_DAT3
MMC2_CMD
MMC2_CLK
MMC2_DAT0
MMC2_DAT1
C157 NO POP
C158 NO POP
C159 NO POP
C160 NO POP
C161 NO POP
C162 NO POP


MEMORY INTERFACE
PERIPHERAL INTERFACE
DB MEMORY/PERIPERAL INTERFACES
EXPANSION BUS CH2
Spectrum Digital Incorporated
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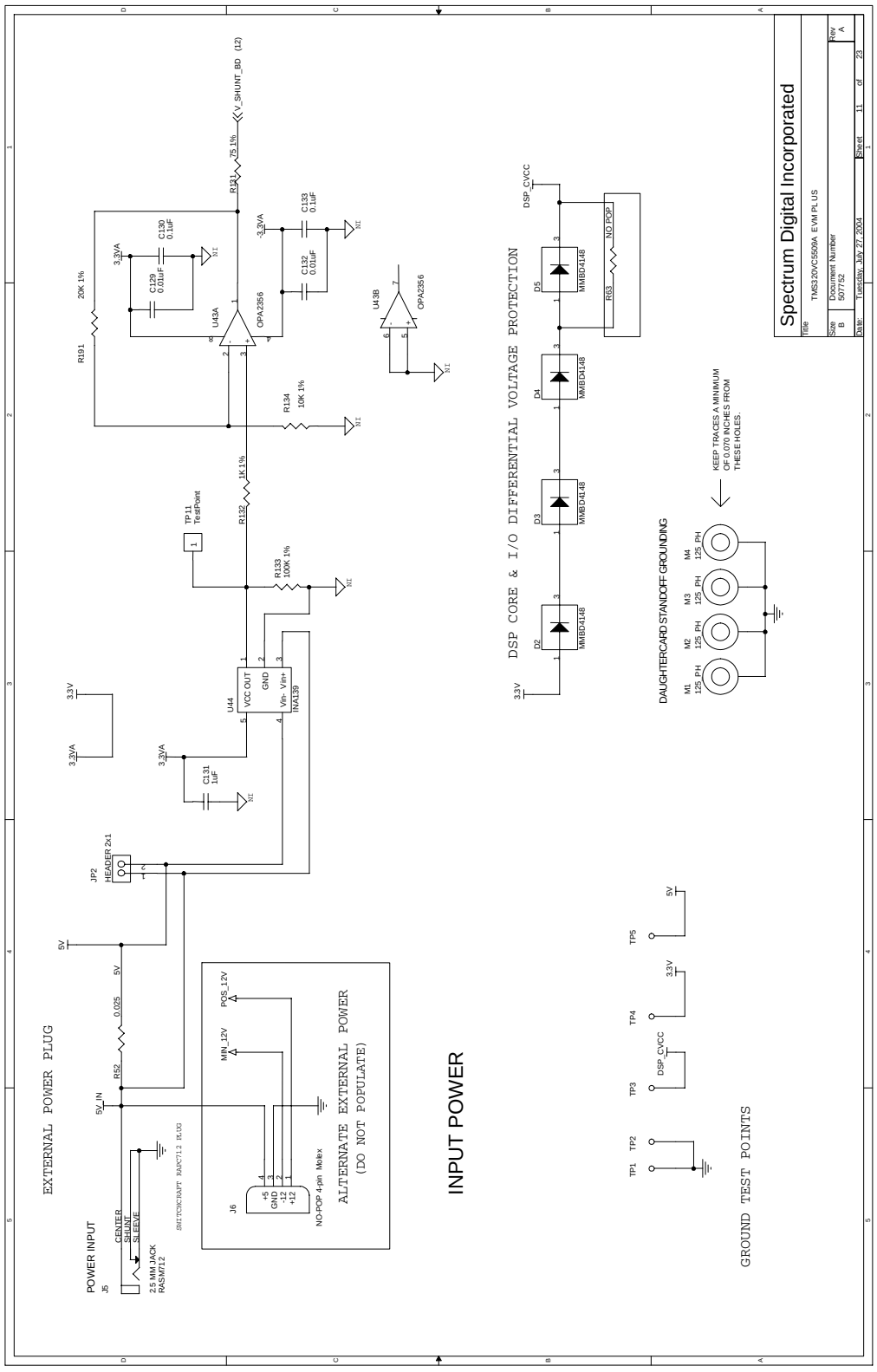
SFM-140-L2-S-D-LC
TPS767330QPWP
P1A
P1B
P2A
P2B
U16
RN17
RN18
R59
R63
R67
R75
C66
C107
X_A[1..20]
X_D[0..15]
X_BE0n
X_BE1n
X_REn
X_OEn
X_CE3n
X_WEn
X_ARDY
X_CE2n
X_RESETn
X_INT1n
X_INT2n
X_INT3n
X_INT4n
X_TOUT0
X_INT0n
X_CLKX1
X_FSX1
X_CLKR1
X_FSR1
X_CLKX2
X_FSX2
X_CLKR2
X_FSR2
X_DX1
X_DR1
X_DX2
X_DR2
X_TIN0
X_CLKOUT
X_ARDY
DC_PORSTn
DC_DETECTn
DC_CNTL0
DC_CNTL1
DC_STAT0
DC_STAT1
3.3V_DB
5V
10K
1uF
10uF


Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
EXTERNAL POWER PLUG
DSP CORE & I/O DIFFERENTIAL VOLTAGE PROTECTION
DAUGHTERCARD STANDOFF GROUNDING
KEEP TRACES A MINIMUM OF 0.070 INCHES FROM THESE HOLES.
INPUT POWER
ALTERNATE EXTERNAL POWER (DO NOT POPULATE)
GROUND TEST POINTS
POWER INPUT
J5
CENTER
SHUNT
SLEEVE
2.5 MM JACK RASM712
SWITCHCRAFT RASM712 BLUE
R52
0.025
5V_IN
5V
3.3V
3.3VA
-3.3VA
JP2
HEADER 2x1
U44
INA139
VCC OUT
GND
Vin- Vin+
U43A
U43B
OPA2356
R191
20K 1%
R134
10K 1%
R132
1K 1%
R133
100K 1%
R131
75 1%
V_SHUNT_BD (12)
C129
0.01uF
C130
0.1uF
C131
1uF
C132
0.01uF
C133
0.1uF
TP11
TestPoint
D2
D3
D4
D5
MMBD4148
R63
NO POP
DSP_CVCC
M1
M2
M3
M4
125 PH
TP1
TP2
TP3
TP4
TP5
J6
+5
GND
-12
+12
NO-POP-4-pin Molex
POS_12V
MIN_12V
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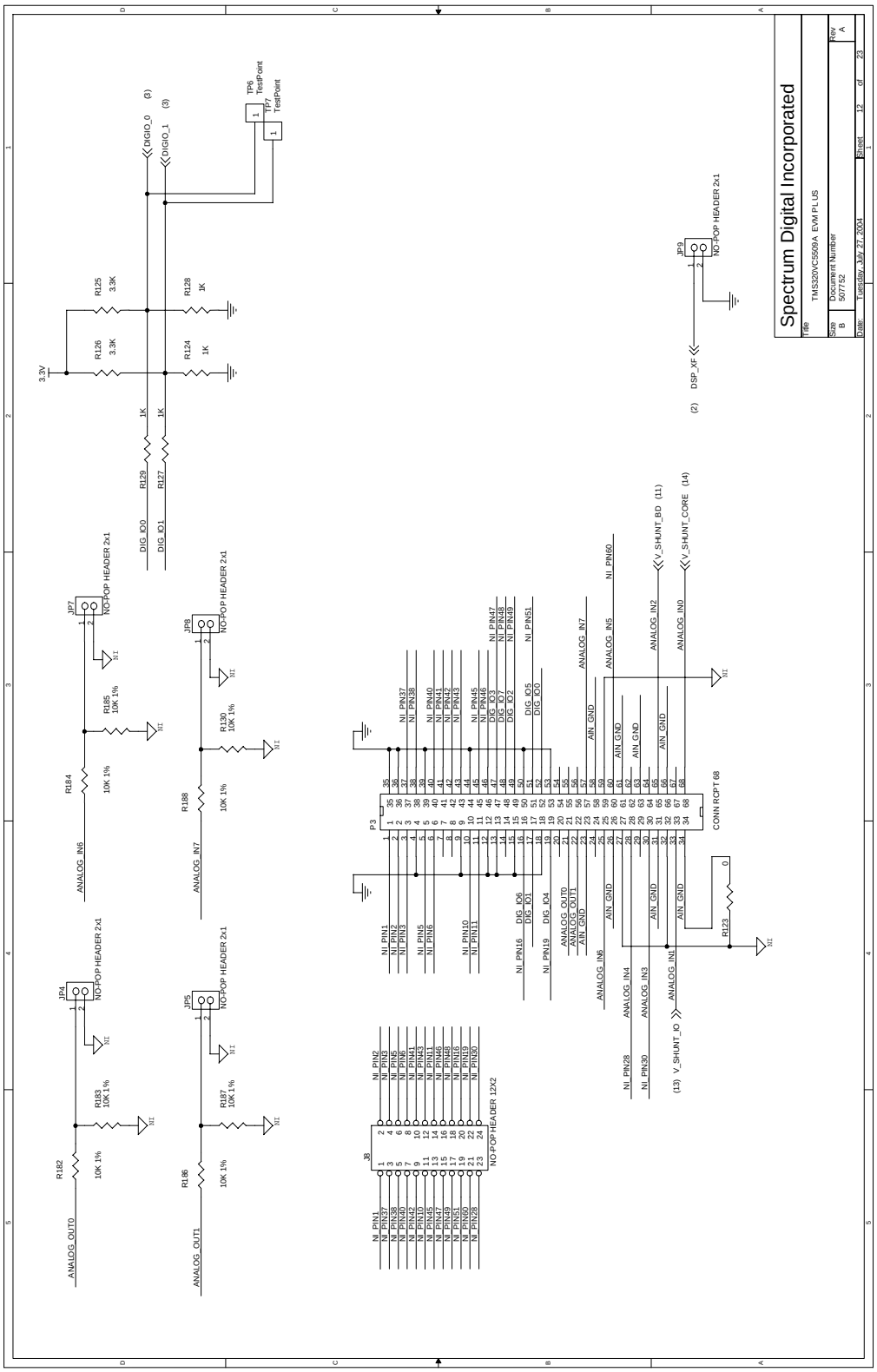
Spectrum Digital Incorporated
TMS320VC5509A EVM PL US
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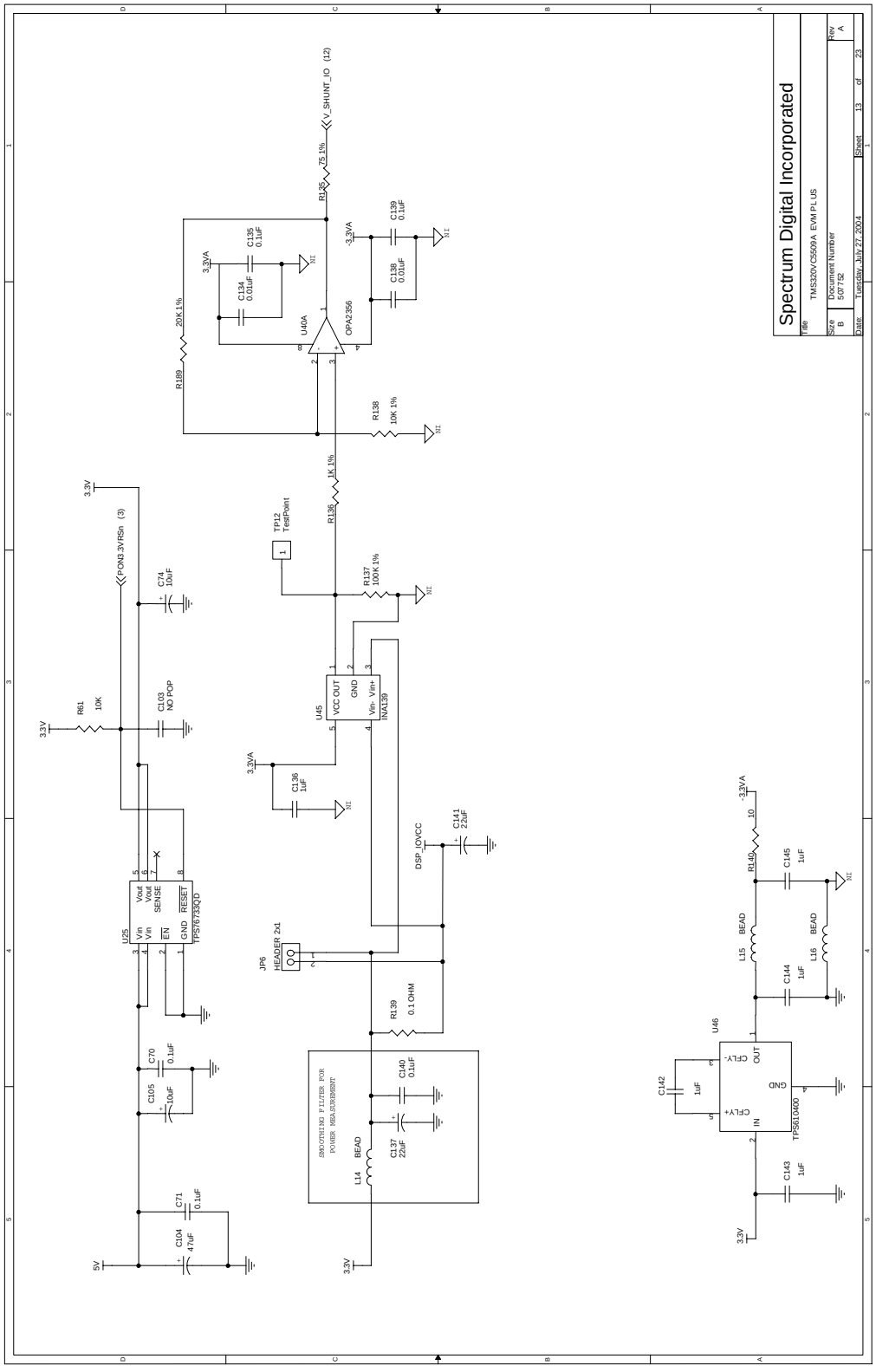
DIGIO_0
DIGIO_1
TP6
TestPoint
3.3V
R125
3.3K
R126
3.3K
R128
1K
R124
1K
R129
1K
R127
1K
DIG_IO0
DIG_IO1
JP7
JP8
JP4
JP5
JP9
NO-POP HEADER 2x1
R185
10K 1%
R130
10K 1%
R184
10K 1%
R188
10K 1%
R183
10K 1%
R187
10K 1%
R182
10K 1%
R186
10K 1%
ANALOG_IN6
ANALOG_IN7
ANALOG_OUT0
ANALOG_OUT1
DSP_XF
R123
0
P3
CONN RCPT 68
J8
NO-POP HEADER 12X2
V_SHUNT_BD
V_SHUNT_CORE
V_SHUNT_IO
AIN_GND
ANALOG_IN0
ANALOG_IN1
ANALOG_IN2
ANALOG_IN3
ANALOG_IN4
ANALOG_IN5
ANALOG_IN7
ANALOG_IN8
DIG_IO3
DIG_IO7
DIG_IO2
DIG_IO5
DIG_IO0
DIG_IO6
DIG_IO1
DIG_IO4
NI_PIN1
NI_PIN2
NI_PIN3
NI_PIN5
NI_PIN6
NI_PIN10
NI_PIN11
NI_PIN16
NI_PIN19
NI_PIN28
NI_PIN30
NI_PIN35
NI_PIN36
NI_PIN37
NI_PIN38
NI_PIN39
NI_PIN40
NI_PIN41
NI_PIN42
NI_PIN43
NI_PIN45
NI_PIN46
NI_PIN47
NI_PIN48
NI_PIN49
NI_PIN51
NI_PIN60
NI_PIN61
NI_PIN62
NI_PIN63
NI_PIN64
NI_PIN65
NI_PIN66
NI_PIN67
NI_PIN68
NO-POP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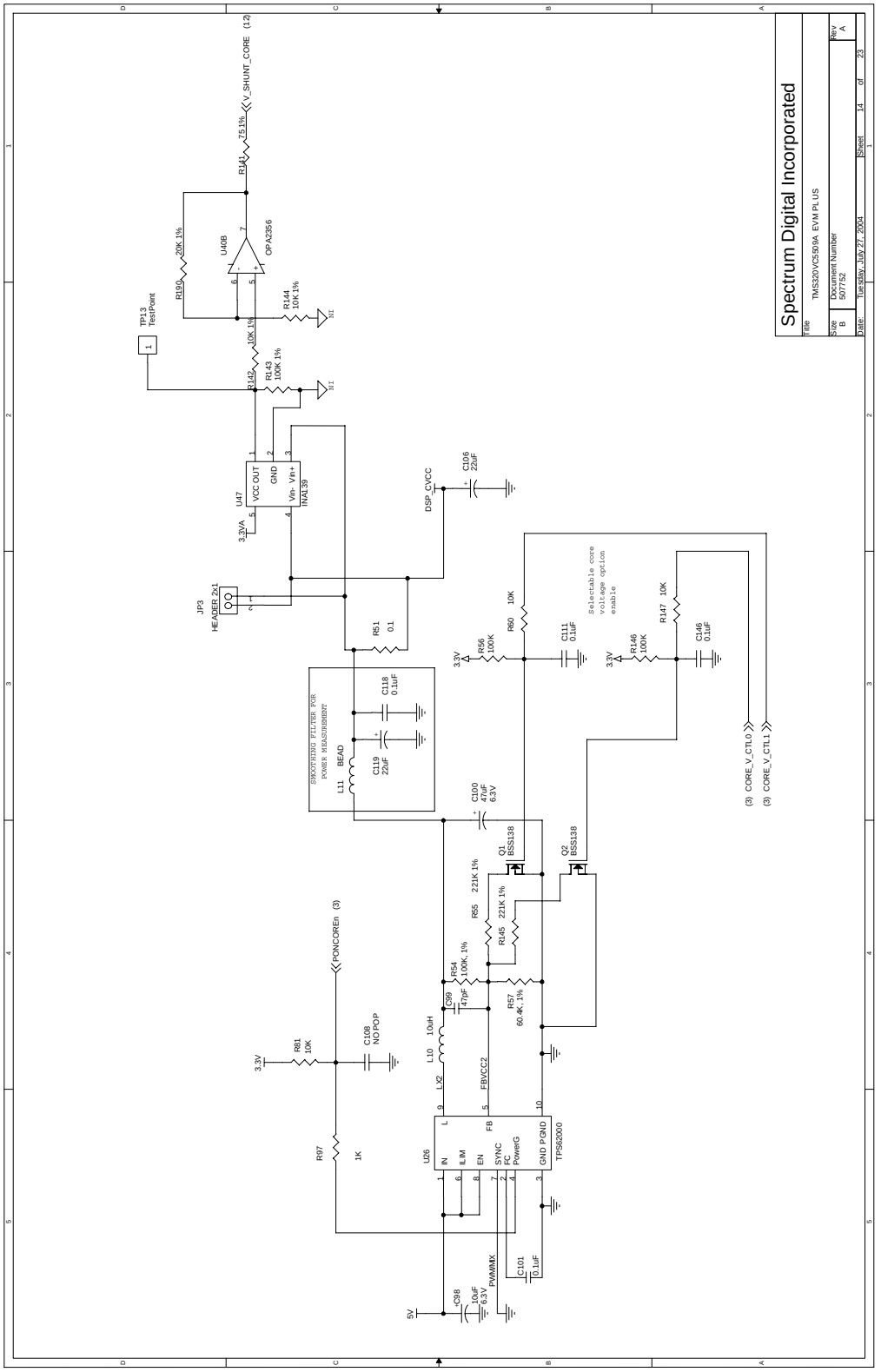
23
V_SHUNT_IO (12)
R135
25 1%
C139
0.1uF
-3.3VA
3.3VA
C135
0.1uF
C134
0.01uF
C138
0.01uF
U40A
OPA2356
20K 1%
R189
R138
10K 1%
1K 1%
R136
TP12
TestPoint
R137
100K 1%
3.3V
(POR)3.3VRSn (3)
C74
10uF
R61
10K
C103
NO POP
U45
VCC OUT
GND
Vin- Vin+
INA139
C136
1uF
U25
Vout
Vout
SENSE
Vin
Vin
EN
GND
RESET
TPS76733QD
C70
0.1uF
C105
10uF
C71
0.1uF
C104
47uF
5V
JP6
HEADER 2x1
DSP_IOVCC
C141
22uF
R139
0.1 OHM
SMOOTHING FILTER FOR
POWER MEASUREMENT
C140
0.1uF
C137
22uF
L14
BEAD
R140
10
C145
1uF
L15
BEAD
L16
BEAD
C144
1uF
U46
CFLY-
OUT
GND
CFLY+
IN
TPS61040
C142
1uF
C143
1uF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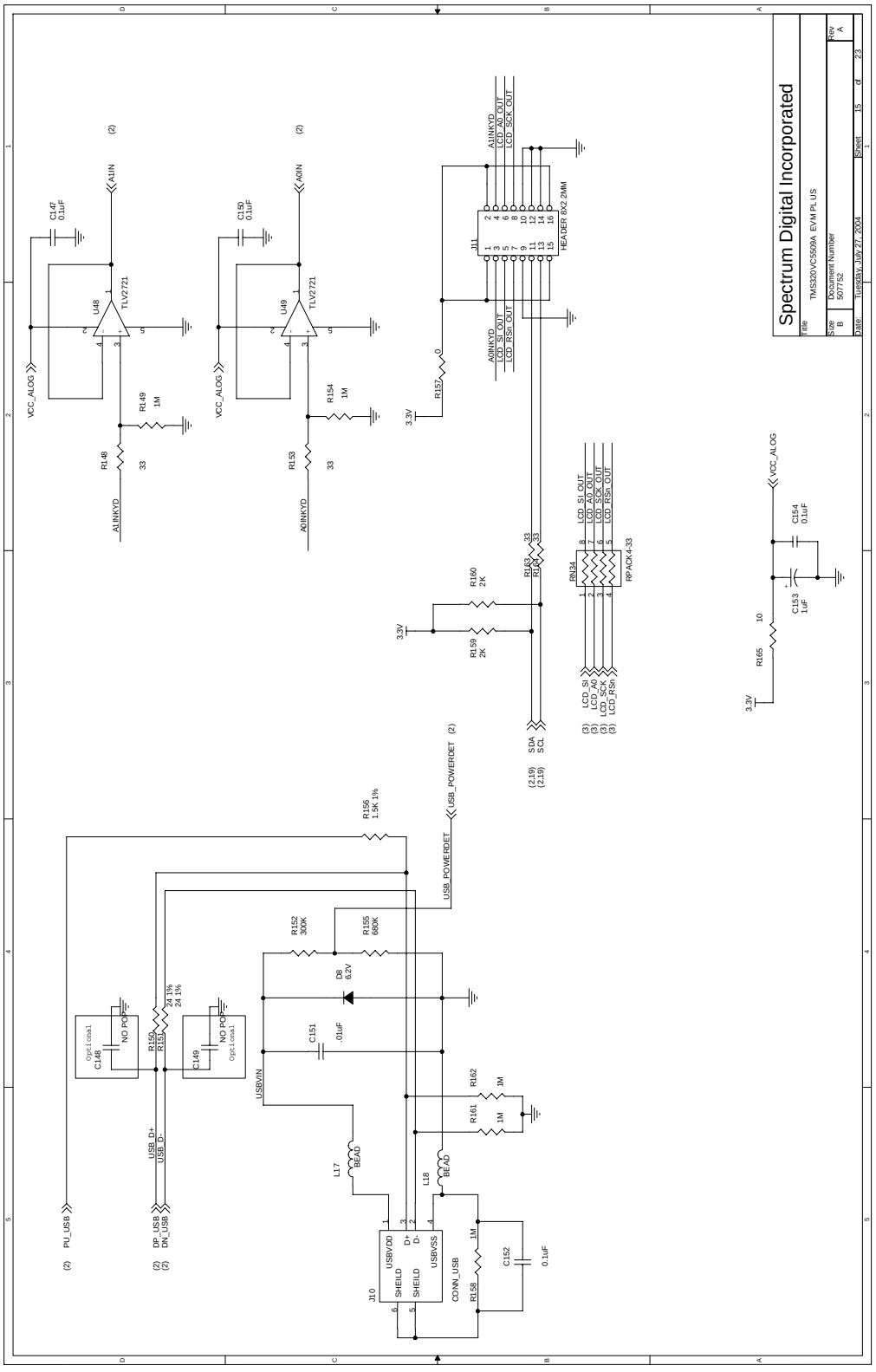
Rev A
V_SHUNT_CORE (12)
R141 .75 1%
U40B
OPA2356
R190 20K 1%
R144 10K 1%
R142 10K 1%
R143 100K 1%
TP13 TestPoint
U47
VCC OUT
GND
Vin- Vin+
INA139
3.3VA
JP3 HEADER 2x1
C106 22uF
DSP_CVCC
R51 0.1
C118 0.1uF
C119 22uF
L11 BEAD
SMOOTHING FILTER FOR POWER MEASUREMENT
R60 10K
R56 100K
C111 0.1uF
R146 100K
R147 10K
C146 0.1uF
Selectable core voltage option enable
3.3V
(3) CORE_V_CTL0
(3) CORE_V_CTL1
C100 47uF 6.3V
Q1 BSS138
Q2 BSS138
R55 221K 1%
R145 221K 1%
R54 100K 1%
R57 60.4K 1%
C99 47pF
L10 10uH
R81 10K
C108 NOPOP
PONCOREn (3)
R97 1K
U26
TPS62000
IN
ILIM
EN
SYNC
PC
PowerG
GND PGND
L
FB
LX2
FBVCC2
C101 0.1uF
C38 10uF 6.3V
PWMMX
5V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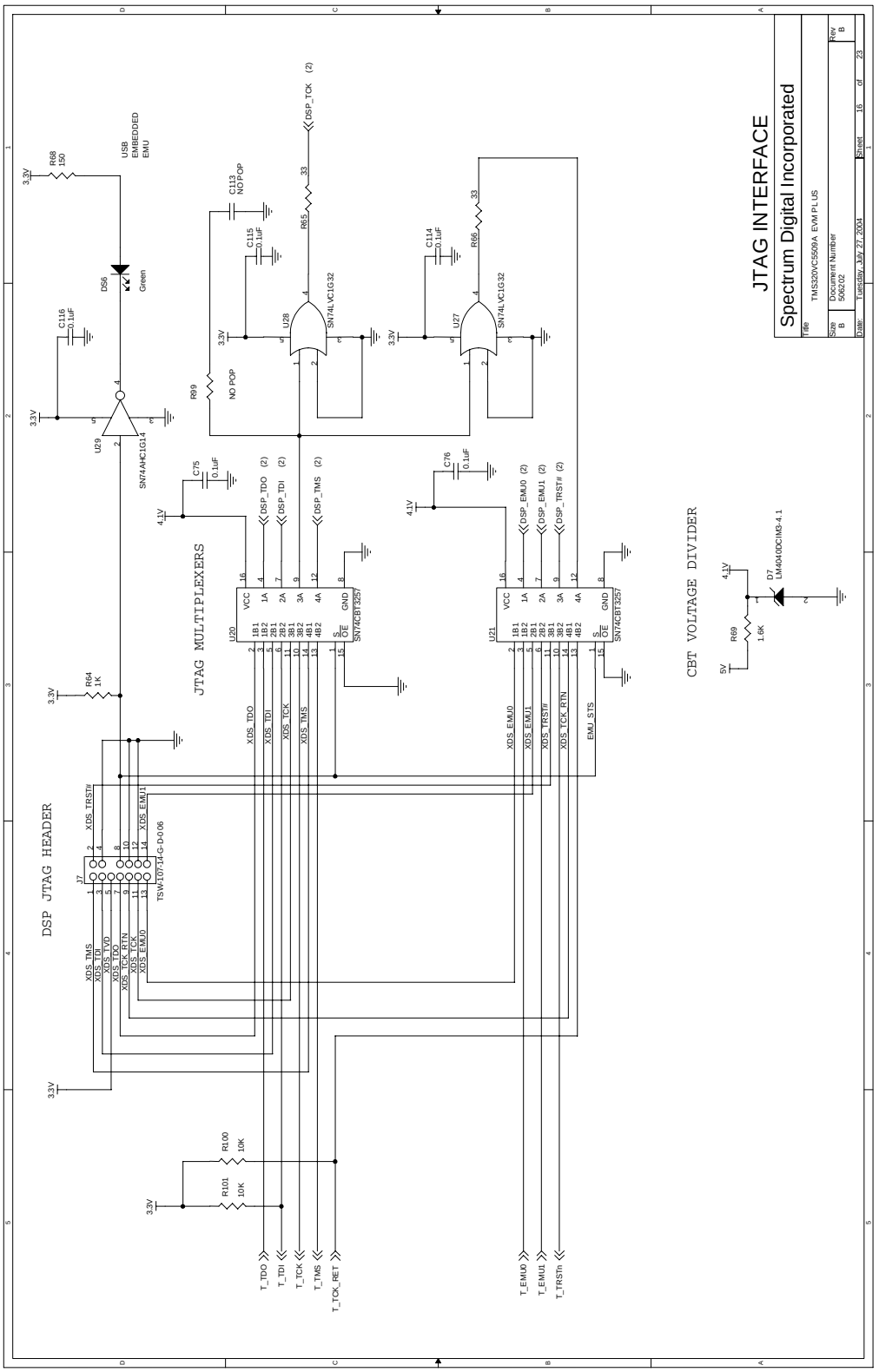
U48
TLV2721
U49
TLV2721
C147
0.1uF
C150
0.1uF
R149
1M
R154
1M
R148
33
R153
33
R157
0
R156
1.5K 1%
R152
300K
R155
680K
D8
6.2V
C151
.01uF
R150
24 1%
R151
24 1%
C148
NO POP
C149
NO POP
R162
1M
R161
1M
L17
BEAD
L18
BEAD
R158
1M
C152
0.1uF
J10
CONN_USB
J11
HEADER 8X2 2MM
R160
2K
R159
2K
R143
33
R144
33
RN34
RPACK-33
C154
0.1uF
C153
1uF
R165
10
A1INKYD
A0INKYD
LCD_SI_OUT
LCD_A0_OUT
LCD_SCK_OUT
LCD_RSn_OUT
USB_POWERDET
USBVIN
USB_D+
USB_D-
VCC_ALOG
A1IN
A0IN
3.3V
SDA
SCL


JTAG INTERFACE
Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
Document Number
506202
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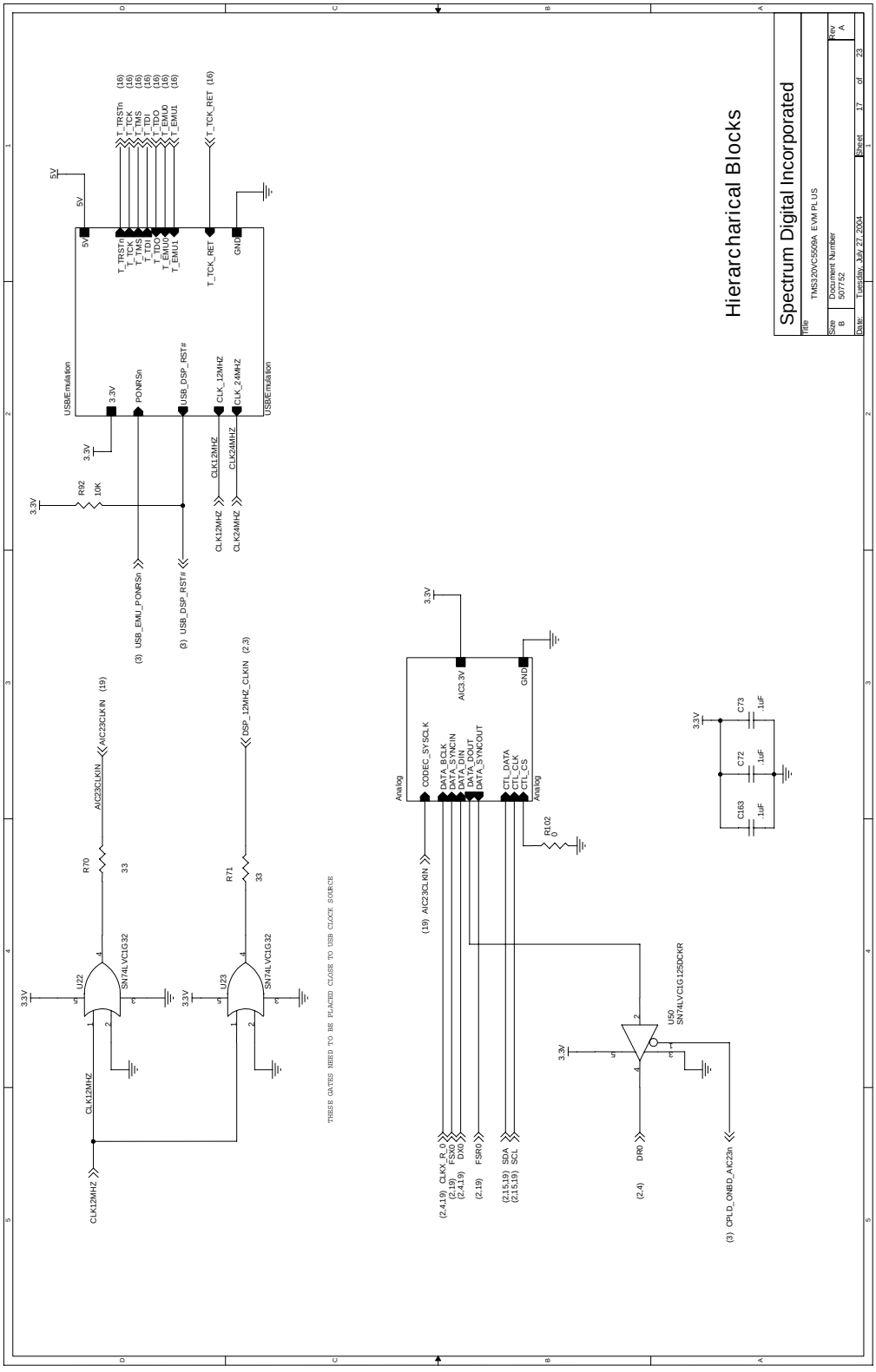
DSP JTAG HEADER
JTAG MULTIPLEXERS
CBT VOLTAGE DIVIDER
TSW-107-14-G-D-006
SN74AHC1G14
SN74LVC1G32
SN74CBT3257
LM4040CIM3-4.1
USB EMBEDDED EMU
NO POP
XDS_TDO
XDS_TDI
XDS_TCK
XDS_TMS
XDS_EMU0
XDS_EMU1
XDS_TRST#
XDS_TCK_RTN
EMU_STS
DSP_TCK (2)
DSP_TDO (2)
DSP_TDI (2)
DSP_TMS (2)
DSP_EMU0 (2)
DSP_EMU1 (2)
DSP_TRST# (2)
T_TDO
T_TDI
T_TCK
T_TMS
T_TCK_RET
T_EMU0
T_EMU1
T_TRSTn


Hierarcharical Blocks
Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
Document Number
5077S2
Tuesday, July 27, 2004
USBEmulation
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TCK_RET
PONRSn
USB_DSP_RST#
CLK_12MHZ
CLK_24MHZ
R92
10K
(3) USB_EMU_PONRSn
(3) USB_DSP_RST#
CLK12MHZ
CLK24MHZ
AIC23CLKIN
DSP_12MHZ_CLKIN
R70
R71
33
U22
U23
SN74LVC1G32
THESE GATES NEED TO BE PLACED CLOSE TO USB CLOCK SOURCE
Analog
CODEC_SYSCLK
DATA_BCLK
DATA_SYNCIN
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
CTL_DATA
CTL_CLK
CTL_CS
AIC3.3V
GND
R102
0
(19) AIC23CLKIN
(2,4,19) CLKX_R_0
(2,19) FSX0
(2,4,19) DX0
(2,19) FSR0
(2,15,19) SDA
(2,15,19) SCL
(2,4) DR0
(3) CPLD_ONBD_AIC23n
U50
SN74LVC1G125DCKR
C73
C72
C163
.1uF
1uF
.1uF
3.3V
5V
GND
Title
Size
B
Date
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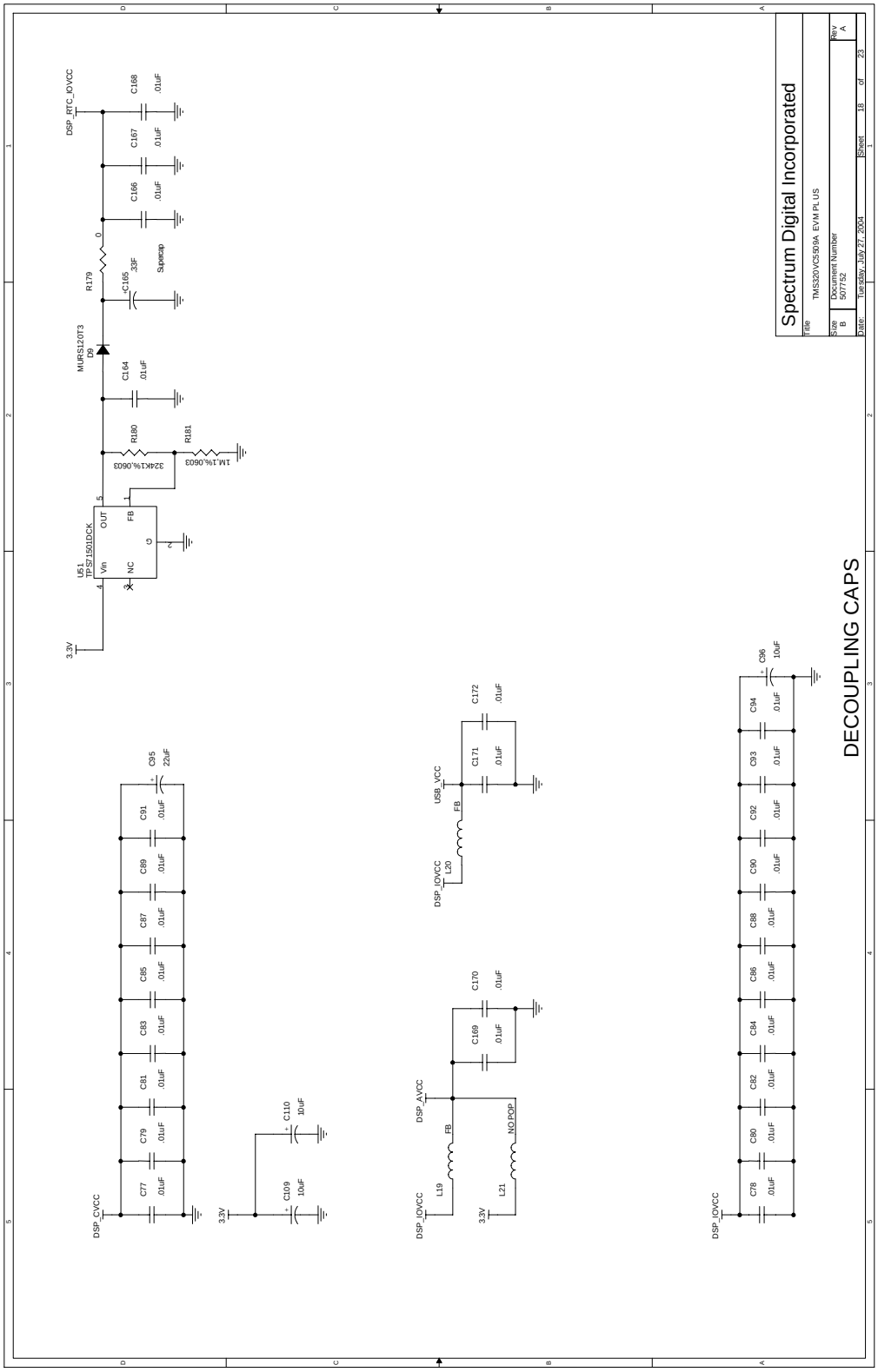
DECOUPLING CAPS
Spectrum Digital Incorporated
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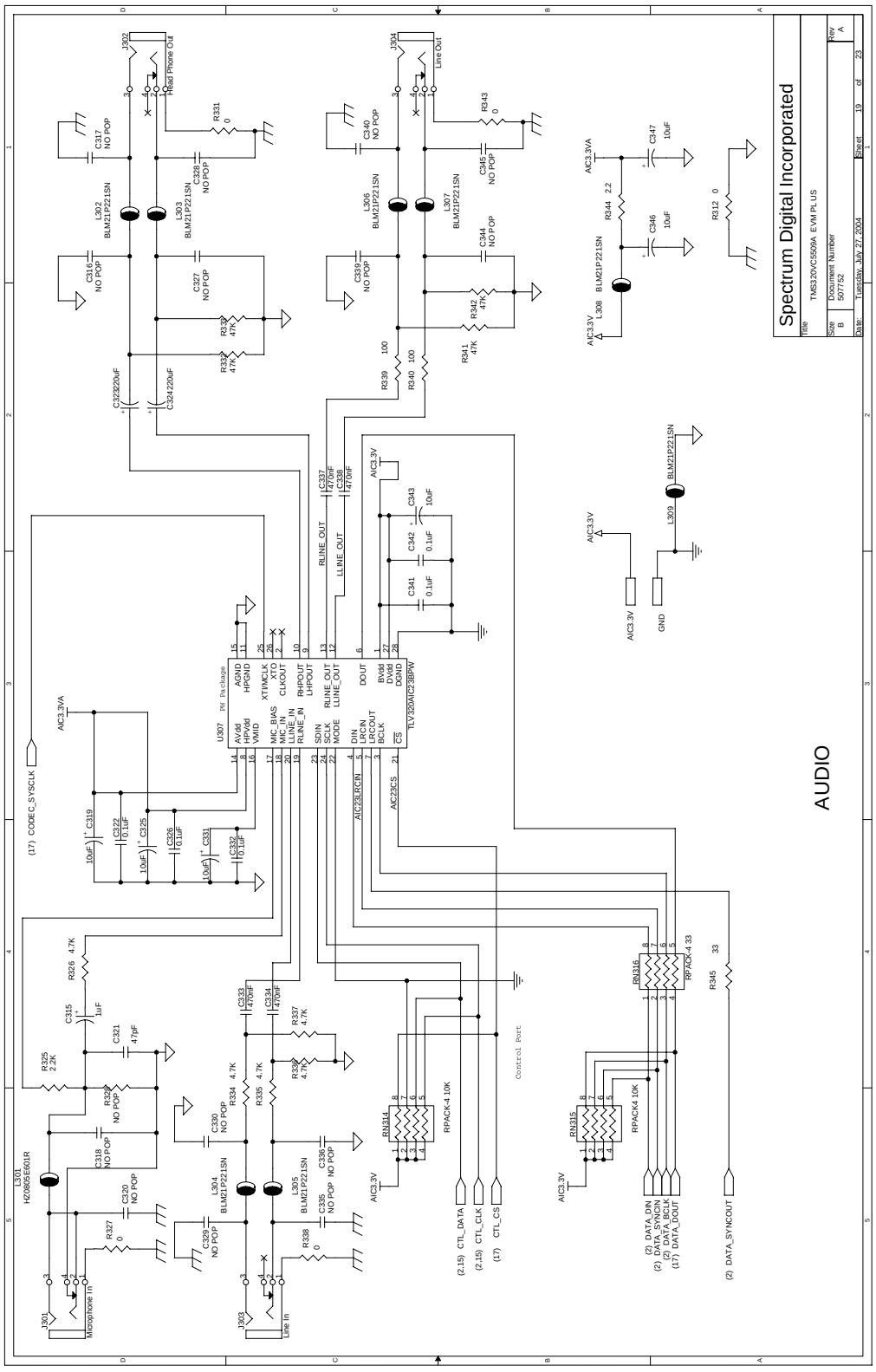
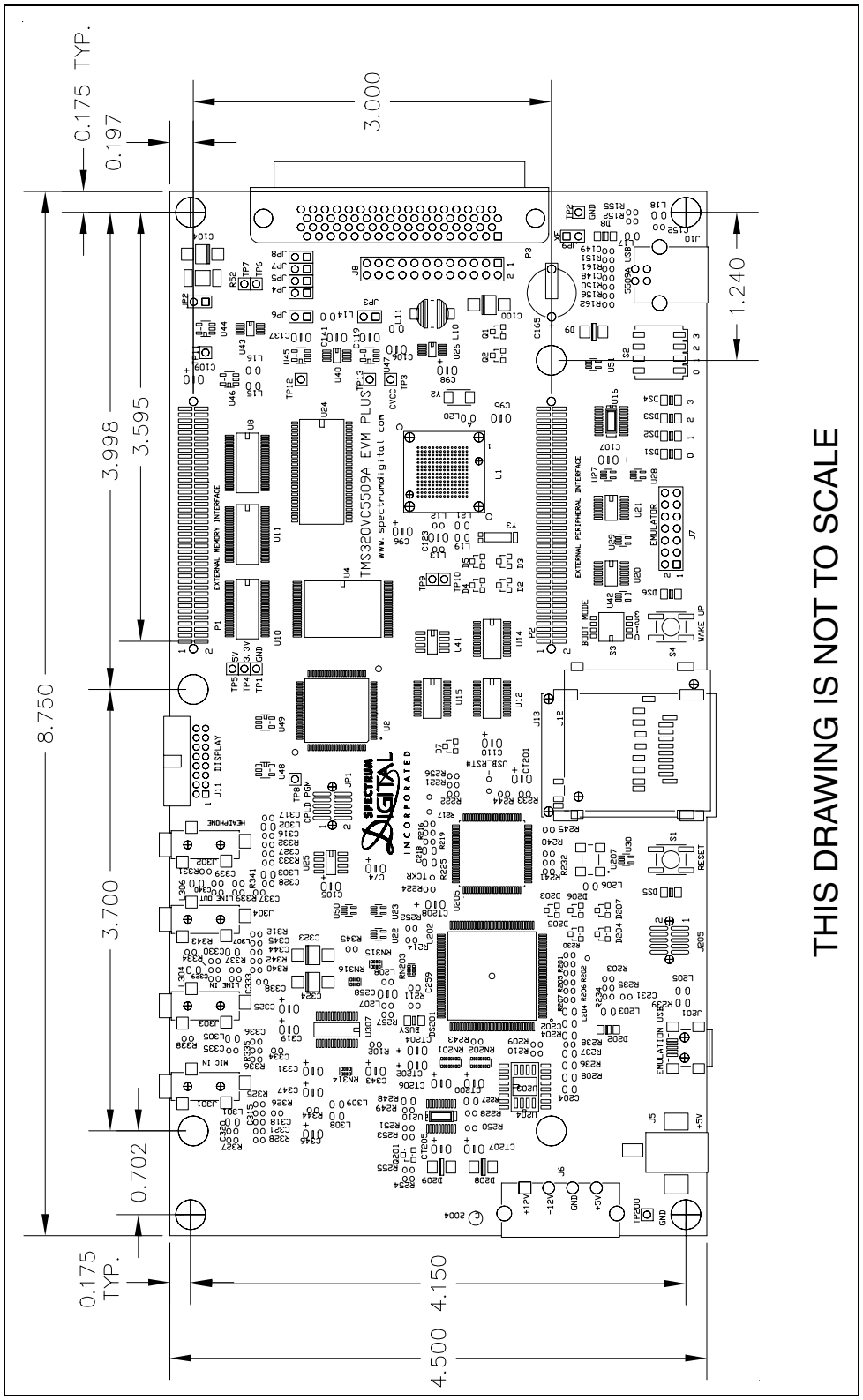
Rev A
DSP_RTC_IOVCC
C168 .01uF
C167 .01uF
C166 .01uF
R179 0
C165 .33F Supercap
MURS120T3 D9
C164 .01uF
R180 324K1%,0603
R181 1M,1%,0603
U51 TPS71501DCK
Vin OUT NC FB GND
3.3V
DSP_CVCC
C77 .01uF
C79 .01uF
C81 .01uF
C83 .01uF
C85 .01uF
C87 .01uF
C89 .01uF
C91 .01uF
C95 220uF
C109 10uF
C110 10uF
DSP_IOVCC
L19 FB
DSP_AVCC
C169 .01uF
C170 .01uF
L21 NO POP
USB_VCC
C171 .01uF
C172 .01uF
L20 FB
C78 .01uF
C80 .01uF
C82 .01uF
C84 .01uF
C86 .01uF
C88 .01uF
C90 .01uF
C92 .01uF
C93 .01uF
C94 .01uF
C96 10uF


AUDIO
Spectrum Digital Incorporated
TMS320VC5509A EVM PLUS
Document Number 507752
Rev A
Tuesday, July 27, 2004
Microphone In
Line In
Head Phone Out
Line Out
TLV320AIC23BPW
Control Port
(17) CODEC_SYSCLK
(2.15) CTL_DATA
(2.15) CTL_CLK
(17) CTL_CS
(2) DATA_SYNCIN
(2) DATA_BCLK
(17) DATA_DOUT
(2) DATA_SYNCOUT

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320VC5509A EVM PLUS produced by Spectrum Digital.


0.175 TYP.
0.197
3.000
1.240
3.998
3.595
8.750
3.700
0.702
0.175
TYP.
4.150
4.500
TMS320VC5509A EVM PLUS
www.spectrumdigital.com
EXTERNAL MEMORY INTERFACE
EXTERNAL PERIPHERAL INTERFACE
BOOT MODE
WAKE UP
EMULATOR
RESET
THIS DRAWING IS NOT TO SCALE

[redacted]

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507755-0001 Rev.A