

TMS320VC5416 Portable Evaluation Platform (PEP)

*Technical
Reference*

TMS320VC5416
Portable Evaluation Platform (PEP)
Technical Reference

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About This Manual

This document describes the board level operations of the TMS320VC5416 Portable Evaluation Module (PEP). The PEP is based on the Texas Instruments TMS320VC5416 Digital Signal Processor. This module is also referred to as the DHP100 DSP Hearing Processor Evaluation Module.

The TMS320VC5416 PEP is a portable card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5416 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5416 will sometimes be referred to as the VC54xx.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC54XX Users Guide
Texas Instruments TMS320VC54XX Fixed Point Assembly Language Users Guide
Texas Instruments TMS320VC54XX Fixed Point C Language Users Guide
Texas Instruments TMS320VC54XX Fixed Point C Source Debugger Users Guide

Chapter 1

Introduction to the TMS320VC5416 Portable Evaluation Platform

Chapter One provides a description of the TMS320VC5416 Portable Evaluation Platform (PEP) along with the key features and a block diagram of the circuit board.

NOTE: The Texas Instruments version of this product is referred to as the DHP100 DSP Hearing Processor Evaluation Module, the DHP100 DSP Hearing Processor EVM Board, or as the DHP100 EVM Board.

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1.0 Overview of the TMS320VC5416 PEP

The TMS320VC5416 Portable Evaluation Platform (PEP) is a battery powered stand-alone card. It allows evaluators to prototype portable audio solutions on the VC5416 digital signal processor (DSP) to determine if it meets their application requirements.

The C5416 PEP is shipped with a TMS320VC5416 processor. The PEP allows full speed verification of C5416 code. With 16K words of on-chip memory, 256K words Flash ROM, and a TLC320AIC23 Sigma Delta codec, the board can solve a variety of problems as shipped. One expansion connector is provided for any necessary evaluation of other codecs not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a number of user interfaces are provided. Debuggers providing assembly language and 'C' high level language debug are available with JTAG emulators.

1.1 Key Features of the TMS320VC5416 PEP

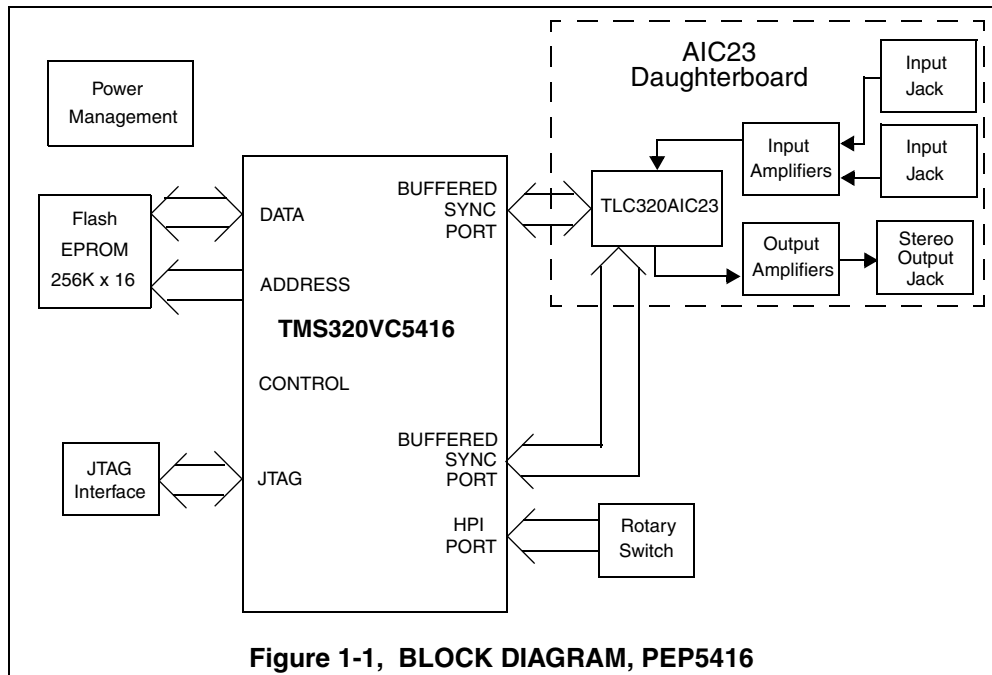
The C5416 PEP has the following features:

- TMS320VC5416 operating at 12-96 MHz
- TLV320AIC23 Sigma Delta Codec daughterboard with stereo jack input and outputs
- Adjustable input and output amplifiers
- 8 position user selectable rotary switch
- 256K words of onboard Flash ROM
- Expansion Connector for 2 McBSPs
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- Battery Operation or external +5.0 Volt power supply operation
- Plastic enclosure

1.2 Functional Overview of the TMS320VC5416 PEP

Figure 1-1 shows a block diagram of the basic configuration for the C5416 PEP. The major interfaces of the PEP include the target Flash ROM interface, sigma delta codec, and expansion interface.

The C5416 interfaces to 256K words of onboard flash memory. An expansion connector supports an optional synchronous serial port interface. Stereo jacks provide input and outputs to and from the AIC23 codec.



Chapter 2

Operation of the TMS320VC5416 Portable Evaluation Platform

This chapter describes the operation of the TMS320VC5416 Portable Evaluation Platform, the key interfaces and an outline of the circuit board.

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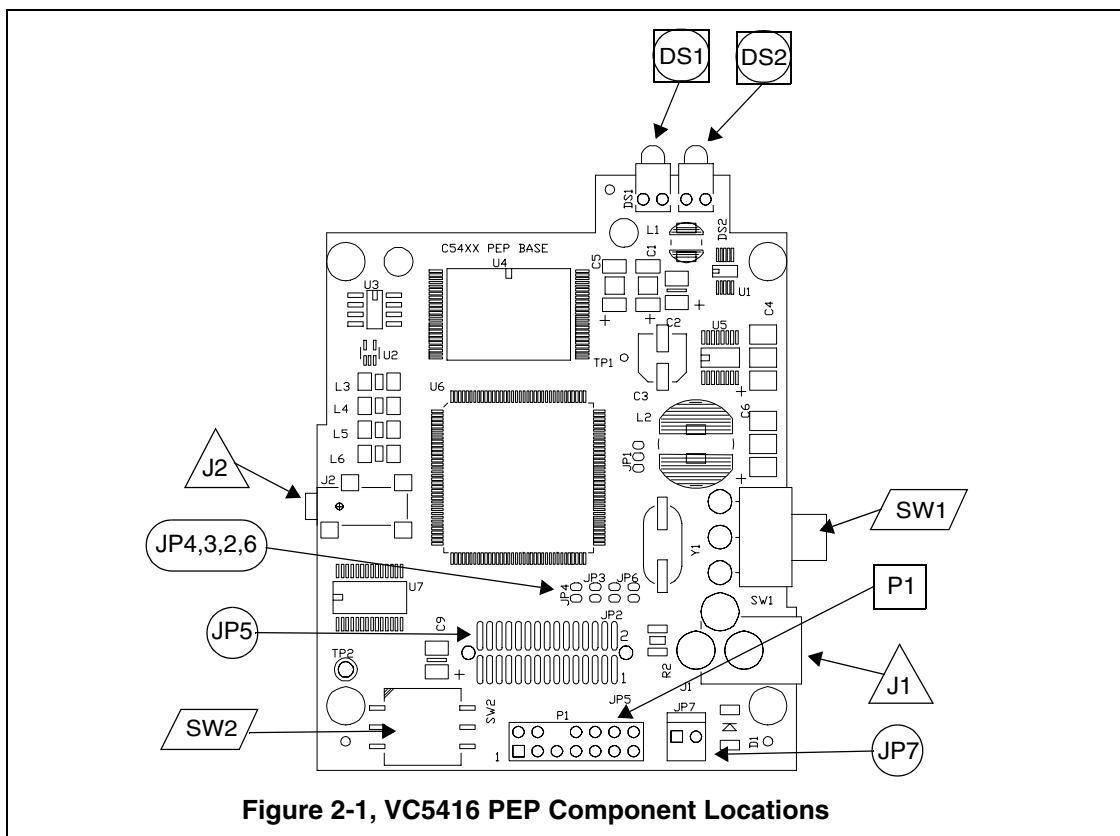
2.0 The TMS320VC5416 PEP Operation

This chapter describes the C5416 Portable Evaluation Platform (PEP), key components, and how they operate. It also provides information on the PEP's various interfaces. The C5416 PEP consists of five major blocks of logic.

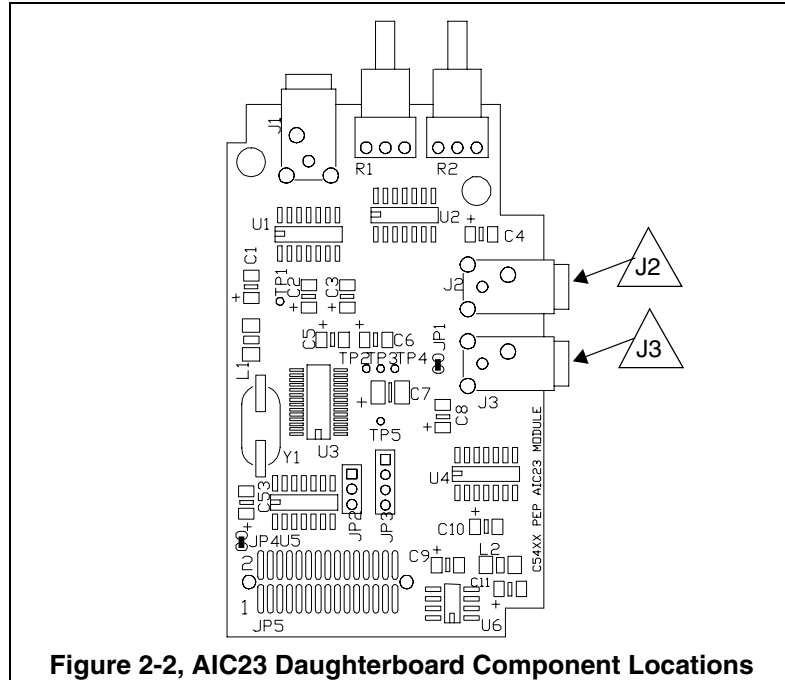
- C5416 external memory
- Analog Interface
- On board Serial I/O interface rotary switch
- Expansion interface
- JTAG Interface

2.1 The TMS320VC5416 PEP Board

The C5416 PEP is a multi-layered printed circuit board which is powered by an external battery or +5 Volt only power supply. Figure 2-1 shows the layout of the C5416 PEP.



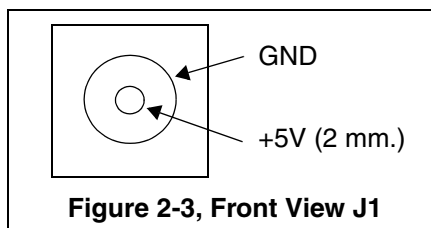
The outline of the AIC23 Daughterboard is shown in the figure below.



2.1.1 Power Connector

The C5416 is powered by a +5.0 Volt only power supply which is available with the module. The board requires a maximum of 150 milliamps. The power is supplied via 2.0 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board regulators provide +5V, -3.3V, +3.3V, and 1.8 volts to the lower voltage components.

The card edge view of the power connector is shown in the figure below.



2.2 TMS320VC5416 Memory Interface

The PEP includes 256K words of on board Flash ROM. This Flash ROM is mapped into both program and data memory spaces.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your PEP card please refer to Texas Instruments TMS320VC5416 Users Guide. Furthermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Software Wait State Generation Register(SWWSR). To obtain one waitstate off-chip memory bits in the SWWSR must be appropriately programmed. The board powers up with 7 wait-states. The PEP board does not generate wait states via the ready signal.

2.2.1 Program Memory

There are two configurations for program memory. The selection of these configurations is done by the 5416's OVLY bit in conjunction with the MP/MC- pin. When in OVLY mode, addresses 0x0000 - 0x8000 are internal for every page. In this mode, there are eight (8) 32K word pages of external program Flash ROM. When in linear mode program memory is mapped to external Flash ROM. Shown below are the two program memory configurations.

This unit is designed to boot in microcontroller mode then switch to overlay mode to move programs from external Flash to internal memory to execute at full speed.

Linear Mode, OVLY = 0		Overlay Mode, OVLY = 1	
Hex		Hex	
0x000000	Flash Page 0 Image	0x000000	Reserved
0x00007F		0x00007F	
0x000080	Flash Page 0 Image	0x000080	Internal
0x007FFF		0x007FFF	DARAM
0x008000	Page 0	0x008000	Page 0
0x00FF7F	Flash Page 0	0x00BFFF	* External Flash Page 0
0x00FF80	Page 0	0x00C000	Page 0
0x00FFFF	Flash Page 0 Interrupts External RAM	0x00FFFF	* External Flash Page 0, MP/MC=1 Internal ROM MP/MC=0
0x010000	Page 1	0x018000	Page 1
0x017FFF	Flash Page 1	0x01FFFF	* External Flash Page 1, MP/MC=1 Internal DARAM MP/MC=0
0x018000	Page 1	0x028000	Page 2
0x01FFFF	Flash Page 1 External MP/MC=1 Internal MP/MC=0	0x02FFFF	* External Flash Page 2, MP/MC=1 Internal DARAM MP/MC=0
0x020000	Page 2	0x038000	Page 3
0x027FFF	External Flash Page 2	0x03FFFF	* External Flash Page 3, MP/MC=1 Internal DARAM MP/MC=0
0x028000	Page 2	0x048000	Page 4
0x02FFFF	External Flash Page 2, MP/MC=1 Internal SRAM MP/MC=0	0x04FFFF	External Flash Page 4
0x030000	Page 3	0x058000	Page 5
0x037FFF	External Flash Page 3	0x05FFFF	External Flash Page 5
0x038000	Page 3	0x068000	Page 6
0x03FFFF	Internal MP/MC=1 External Flash Page 3, MP/MC=0	0x06FFFF	External Flash Page 6
0x048000	Page 4	0x078000	Page 7
0x04FFFF	External Flash Page 4	0x07FFFF	External Flash Page 7
0x058000	Page 5		
0x05FFFF	External Flash Page 5		
0x068000	Page 6		
0x06FFFF	External Flash Page 6		
0x078000	Page 7		
0x07FFFF	External Flash Page 7		

Figure 2-4, VC5416 PEP Program Space

2.2.2 Data Memory

The data memory configuration is shown below. The external data memory is mapped from 0x8000 to 0xFFFF.

Figure 2-5 shows the data space memory map for the VC5416 DSP used in the PEP.

Hex	
0x0000 0x005F	Memory-Mapped Registers
0x0060 0x007F	Scratch Pad RAM
0x0080 0x1FFF	8K Dual Access RAM (DARAM)
0x2000 0x7FFF	Single Access RAM (SARAM)
0x8000 0xFFFF	FLASH ROM (DROM=0)

Figure 2-5, VC5416 PEP Data Space

2.3 CPU Oscillator Selection

The TMS320VC5416 PEP is equipped with a 12 Megahertz oscillator. When the processor resets the PLL Clock Module defaults to 12 Mhz CLKOUT in divide mode. The PLL can then be programmed to obtain a variety of clock frequencies. If the PLL frequency is required to change after the programming the part must be returned to the divide mode before the programming of the new PLL frequency. The user should refer to the “PLL Clock Module” section in the TMS320VC5416 data sheet for valid clock configurations.

The software supports 96 Mhz. CPU speed to be compatible with the 5402 and 5416. The 5416 can be operated up to 160 Mhz.

2.4 Analog Interface

The C5416 multi-channel buffered serial (McBSP) port 0 is used to access the onboard TLV320AIC23 sigma delta codec. McBSP serial port 1 on the 5402 and serial port 2 on the 5416 is used to access the AIC23's data port.

2.4.1 J2,J3 Analog Inputs, AIC23 Daughterboard

The analog input is driven from two 3.5 mm. jacks. J2 is the left input and J3 is the right input. Both inputs are DC coupled. These two connectors are on the AIC23 daughterboard. The mating connector is shown in the drawing below.

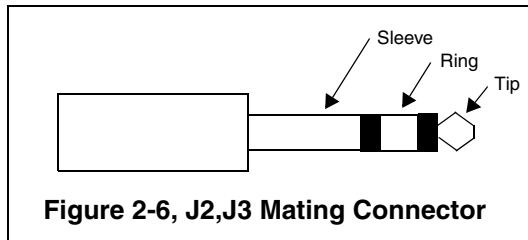


Figure 2-6, J2,J3 Mating Connector

The J2 connector signal definitions are shown in the table below.

Table 1: J2 Signal Definitions

Jack Connector	Signal
Sleeve	Ground
Ring	Microphone Power
Tip	Left Input

The J3 connector signal definitions are shown in the table below.

Table 2: J3 Signal Definitions

Jack Connector	Signal
Sleeve	Ground
Ring	Microphone Power
Tip	Right Input

2.4.2 J2, Analog Output

The analog output is stereo. The mating connector is shown below.

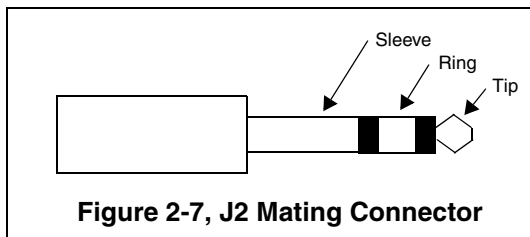


Figure 2-7, J2 Mating Connector

The J2 connector signal definitions are shown in the table below.

Table 3: J2 Signal Definitions

Jack Connector	Signal
Sleeve	Ground
Ring	Right Output
Tip	Left Output

2.5 JP5, I/O Expansion Connector

The TMS320VC5416 PEP has an expansion connector, JP5, which brings out two of the McBSP signals from the DSP. This expansion bus allows the user to design custom circuitry to be used with his application without having to design a CPU card.

This expansion bus is a surface mount double row header. This section contains the signal definitions and pin numbers for this connector.

Table 4: JP5, I/O Expansion Connector

Pin #	Signal	Pin #	Signal
1	+3.3 Volts	2	+3.3 Volts
3	Reserved	4	RESET
5	GND	6	GND
7	BCLKR0	8	BCLKX0
9	BFSR0	10	BFSX0
11	BDR0	12	BDX0
13	GND	14	GND
15	BCLKR1	16	BCLKX1
17	BFSR1	18	BFSX1
19	BDR1	20	BDX1
21	+5 Volts	22	+5 Volts
23	TOUT	24	HPI IO7
25	TOUT1	26	HPI IO6
27	XF	28	HPI IO5
29	CPU I/O Voltage	30	CPU I/O Voltage

2.6 P1, JTAG Interface.

The TMS320VC5416 Evaluation Module is supplied with a 14 pin header interface, P1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-8 below:

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD (+3.3V)	5	6	no pin (key)	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 2-8, JTAG INTERFACE

2.7 Boot Loading With On Chip Bootloader

When configured for on chip boot loading the VC5416 PEP is equipped with 32K words of flash ROM for parallel boot loading. This feature does not disallow the ability to boot from the HPI or serial port, but is intended to allow a convenient method of implementing embedded code on the C5416 evaluation module.

The flash ROM on the evaluation module is mapped in data space from 0x8000 to 0xFFFF when the module is reset. If the module is in microcomputer mode (MP/MC pin = 0) the boot loader will be executed.

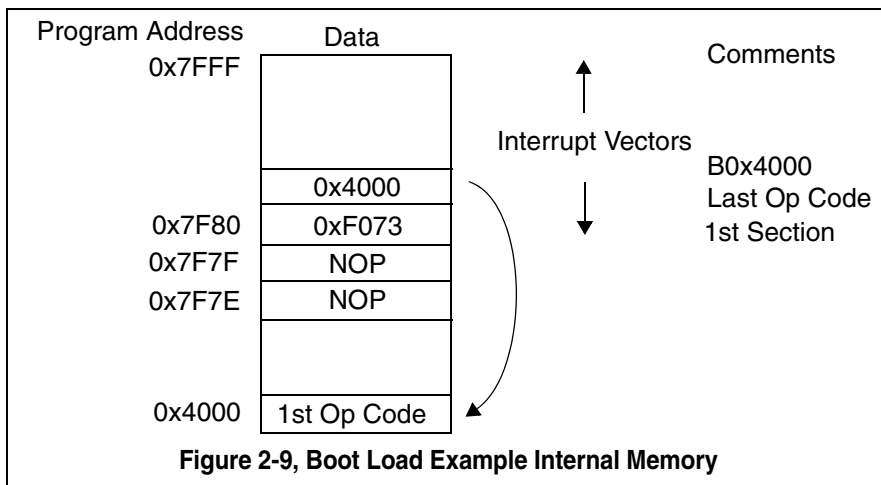
To boot load from flash memory the data must be built in the proper format for the boot loader. Upon execution of the boot loader in parallel mode the on chip boot loader reads the I/O space and/or the data space at 0xFFFF to find the boot loader source address. The appropriate value for the source address boot loading is 0x8000, the flash ROM base address in data space. Since the flash on the evaluation module is word wide we will use the 16 bit parallel load mode in our example.

After the boot loader extracts the source address from the location specified (0xFFFF). The boot loader recognition word (0x10AA) must be located at this address (0x8000 in our example) as shown in table 5.

In our example one section of 0x4000 words will be loaded via the boot loader. Since the part will be in overlay mode on booting our target program space map will be one shown in figure 2-5 in internal C5416 memory.

Table 5: Sample Boot Load Format Stored In Flash ROM

Data Space Address	Data Space Data	Function
0xFFFF	0x8000	Source Address
...	0x0000	Zero Fill
0xC009	0x0000	...
0xC008	0xF495(NOP)	Last Op Code, 1st Section
	0xF495(NOP)	
0x8009		1st Op Code, 1st Section
0x8007	0x4000	Destination Address
0x8006	0x0000	Destination of 1st XPC
0x8005	0x4000	Size of 1st Section
0x8004	0x7F80	Entry Point
0x8003	0x0000	Entry XPC
0x8002	0x8802	BSCR Value
0x8001	0x7FFF	SWWR Value
0x8000	0x10AA	Recognition byte 16 bit mode



In our example one section is loaded. However, if multiple sections are used they are tacked onto the first section in the same format as the first section(0x8005 to 0xC008). Of course, the size of each section is independent, as long as the total size of all the sections is less than 32K words. For more information on boot loading options please refer to the C54xx boot loading document available from Texas Instruments

2.8 VC5416 PEP Jumpers

The PEP320VC5416 has 4 jumpers which determine how features on the PEP are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 6: VC5416 PEP Jumpers

Jumper #	Size	Function
JP6	1 x 2	MP/MC Select
JP2, JP3, JP4	1 x 2	Oscillator Mode Select

Each jumper on the TMS320VC5416 PEP is a 1 x 2 jumper solder pad.

2.8.1 JP6, MP/MC Select

Jumper JP6 is used to enable or disable the on chip bootloader on the TMS320VC5416. The table below shows the two positions and their functions:

Table 7: JP6, Bootload Enable/Disabled

Position	Function
Installed *	Internal Boot Loader Enabled
Open	Internal Boot Loader Disabled

* default

2.8.2 JP2, JP3, JP4, Oscillator Selection

Jumpers JP2, JP3, and JP4 are used together to select different clock modes and speeds for the C5416 DSP. The VC5416 PEP is equipped with a 12 megahertz oscillator.

The C5416 PLL can be configured in one of the two provided clock modes:

- The input clock (CLKIN) is divided; this is called DIV mode
- The input clock (VLKIN) is multiplied by one of 31 possible ratios which range from 0.25 to 15. These ratios are achieved with the Analog Voltage controlled Oscillator (VCO).; this mode is called PLL mode.

When the clock mode is not used, VCO and all the analog parts are disabled in order to minimize the power dissipation

The clock mode can be determined by setting 3 external clock mode pins during reset or by software. In software, a 16 bit register (CLKMD) controls the behavior of the PLL and sets the mode.

At start-up the clock mode is selected with the values on input pins CLKMD1, CLKMD2, and CLKMD3. These these pins are tied to jumpers JP4, JP3, and JP2 respectively.

2.9 LEDs

The VC5416 PEP has two light emitting diodes. Both DS1 and DS2 are under software control. DS1 is connected to the HPI-D3 pin on the DSP. LED DS2 is connected to the HPI-D4 pin on the DSP.

Table 8: LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Green	HPI Data Bit 3	1
DS2	Red	HPI Data Bit 4	1

2.10 Input Amplifier

The inputs can be driven with either standard audio line out voltage or a microphone. JP1 supplies the voltage to power the microphone. Potentiometers R32 and R48 control the gains of the left and right channels respectively.

2.11 Output Amplifier

The outputs have 2 potentiometers that control the output gain. Potentiometers R1 and R2 control the right and left output gains respectively.

2.12 Power Management

SW1 controls the power on or off to the PEP. Power is either supplied from a battery connected to JP1 to an external 2.5 - 5.0 volt DC power supply connected to JP7. On board circuitry generates +5.0, -3.3, +3.3, and core voltage (+1.6 volts for 5416, 1.8. volts for 5402)

2.13 Rotary Switch

The rotary switch SW2 has 16 positions. These positions can be read by the application software on the DSP and used to set or configure parameters in the algorithms, or download different algorithms on power up.

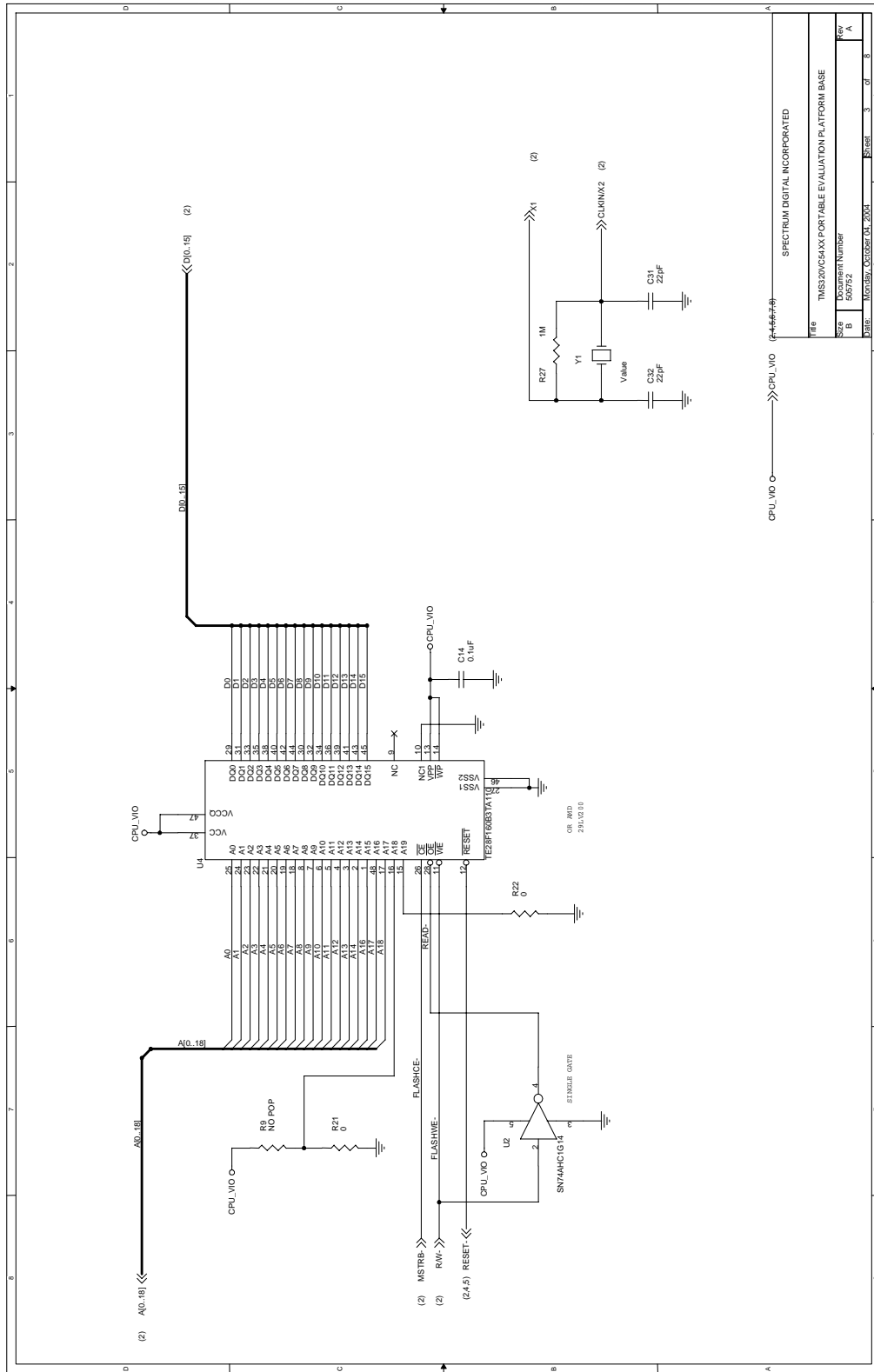
The switch is connected to the Host Port I/O pins HPIO0-HPIO2, which correspond to HD0-HD2 on the VC5416.

Appendix A

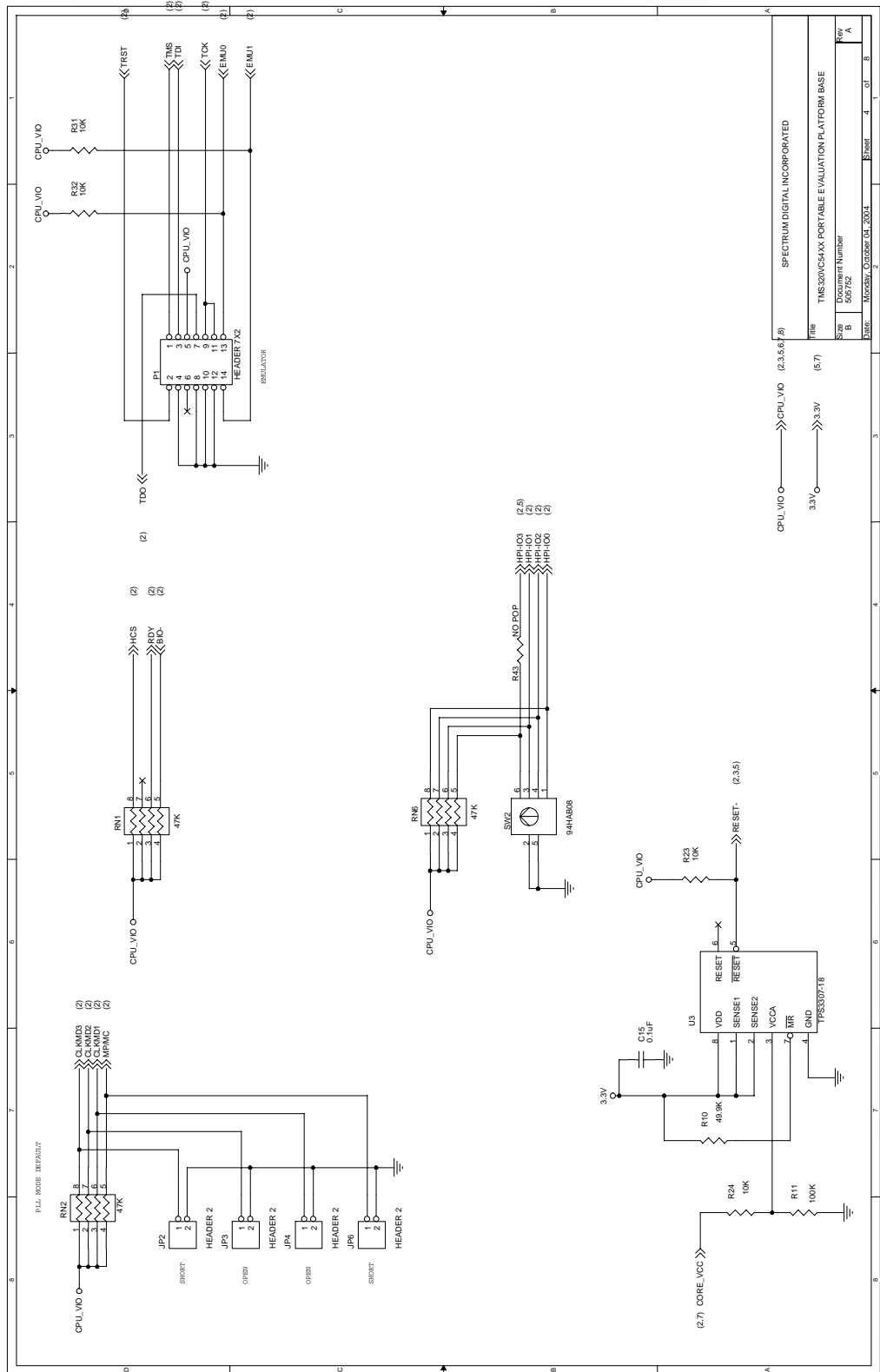
TMS320VC5416 PEP Schematics

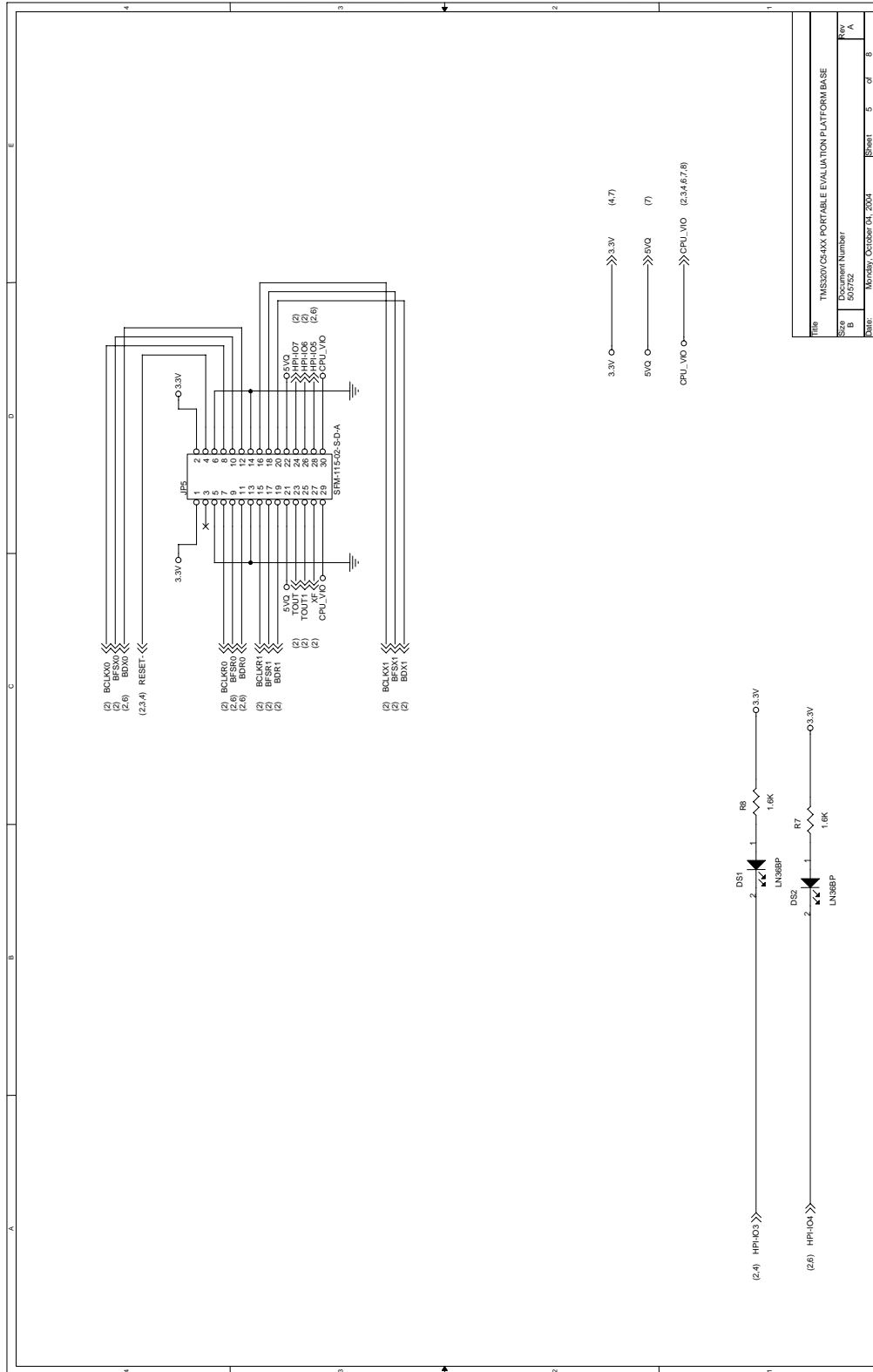
This appendix contains the schematics for the TMS320VC5416 PEP. The schematics were drawn in ORCAD.

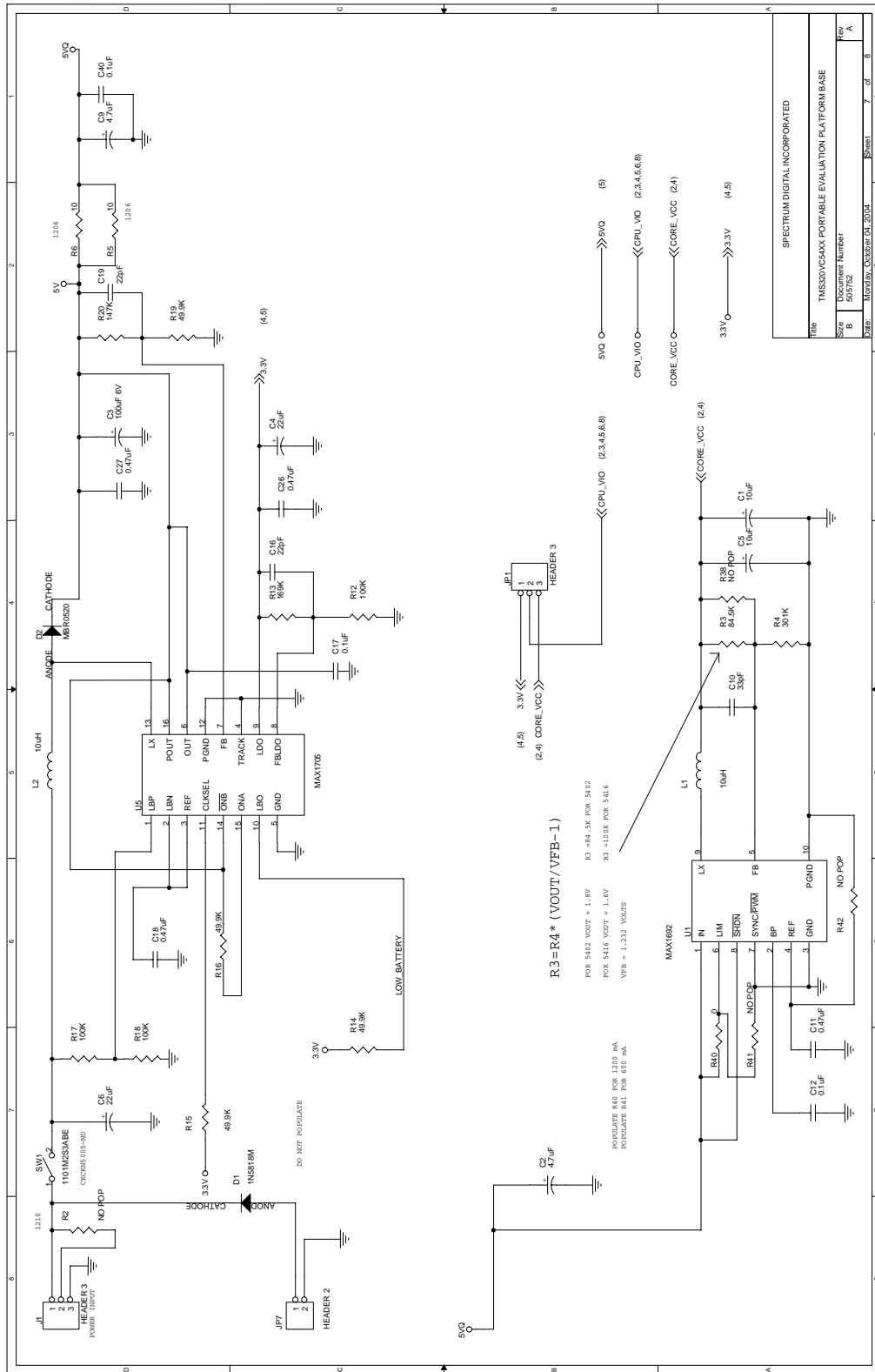
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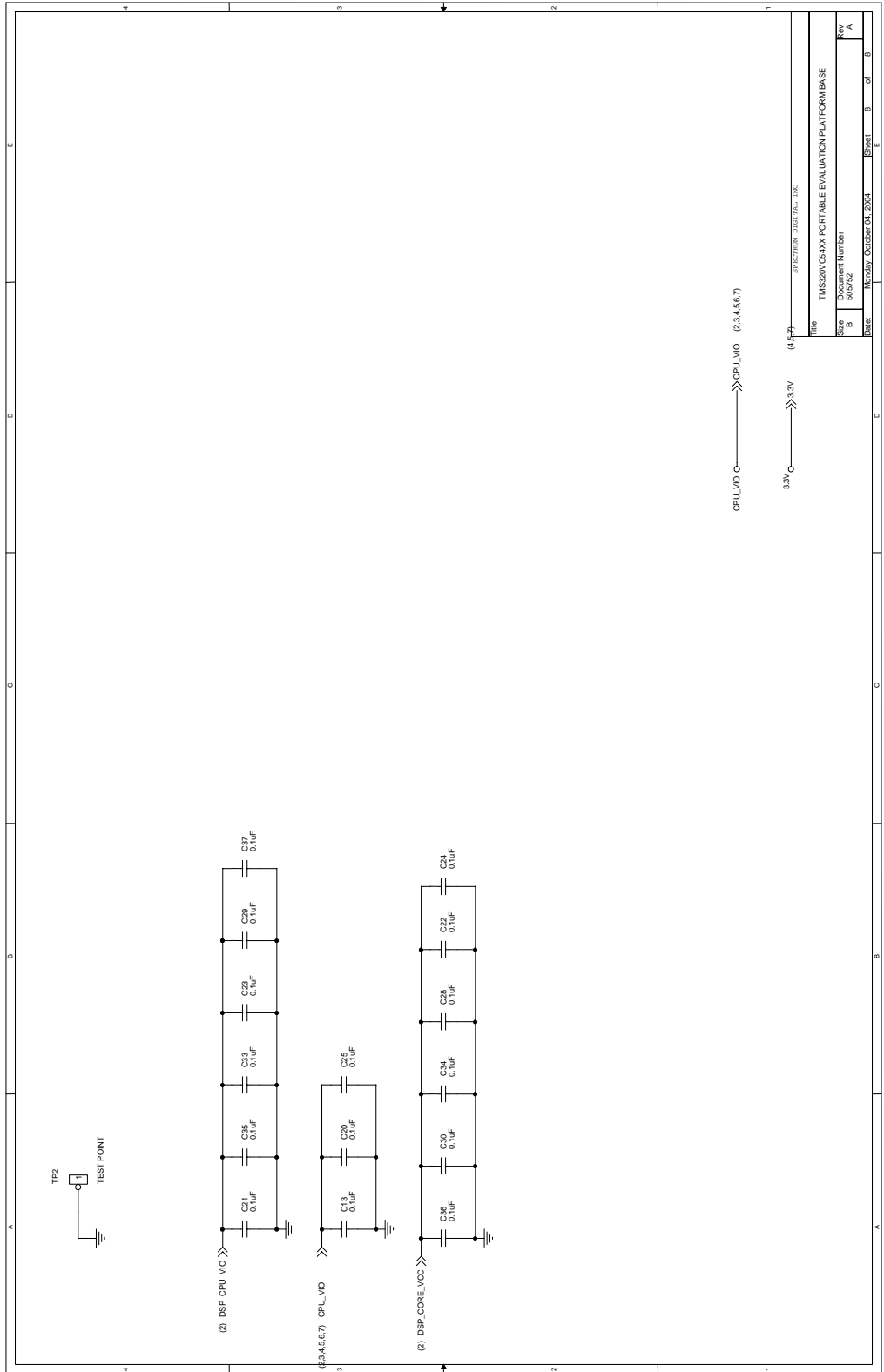


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Size	509/52
Doc Number	Rev A
Year	March, 2001
Sheet	3 of 8









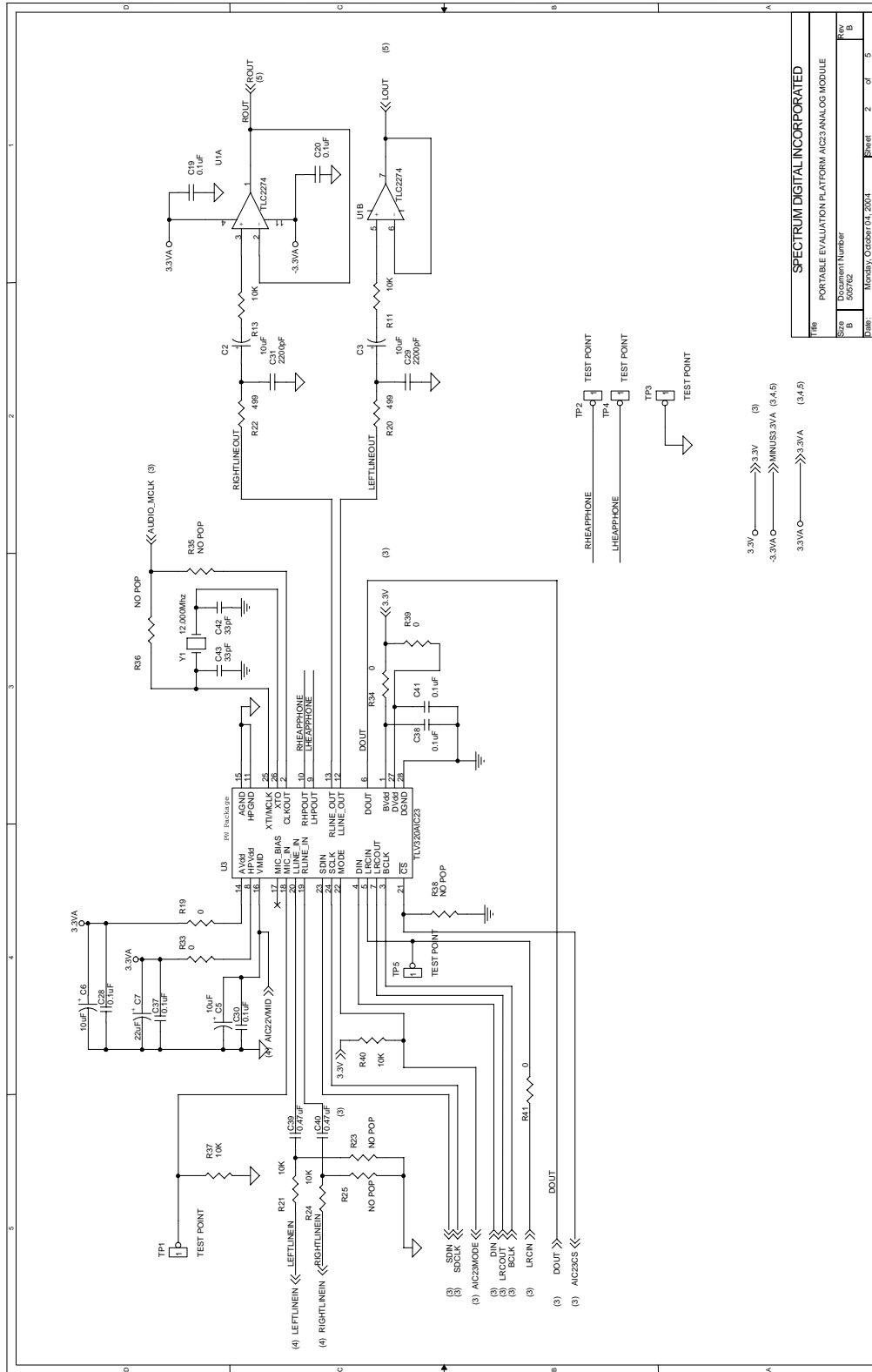
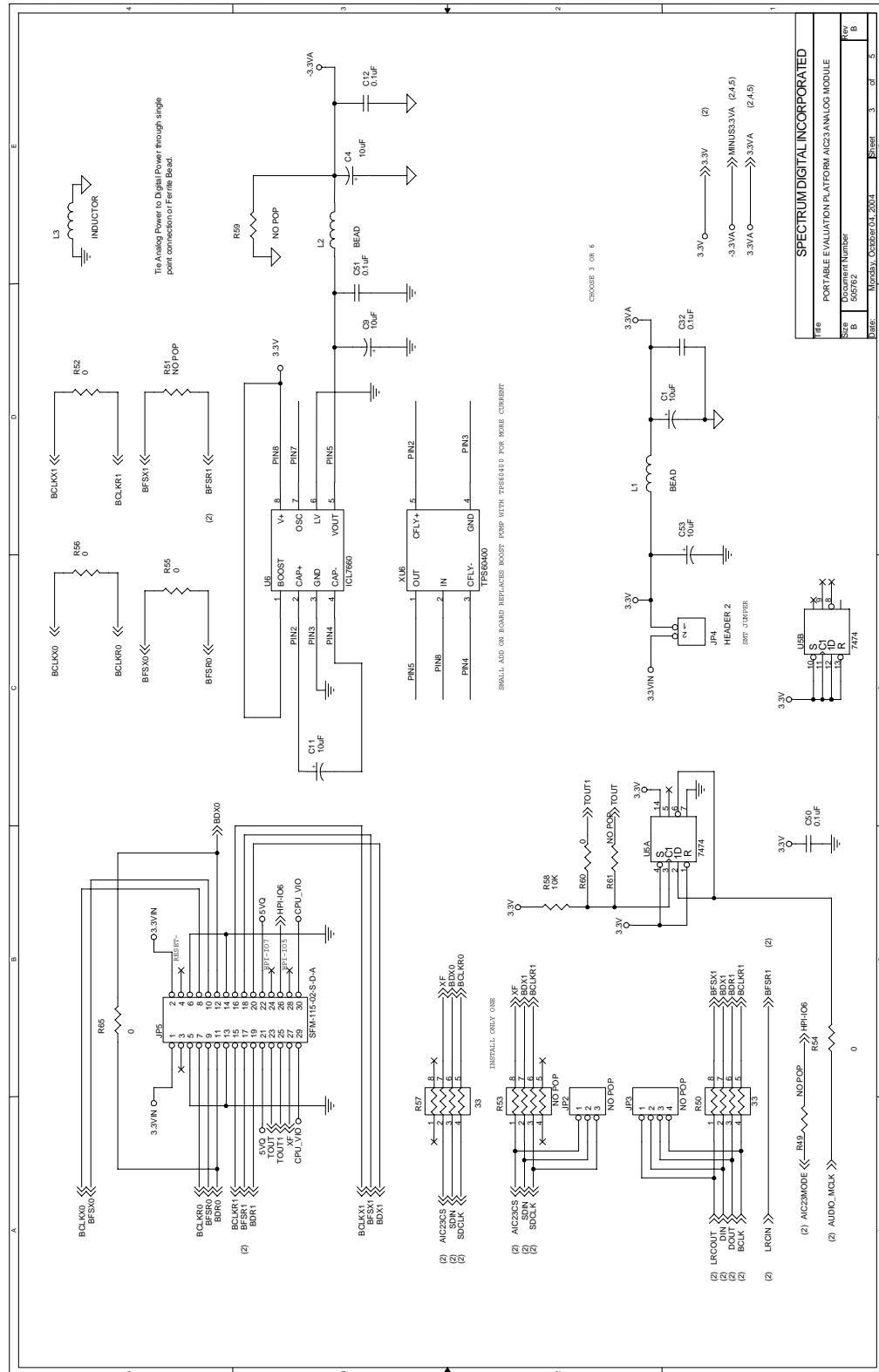
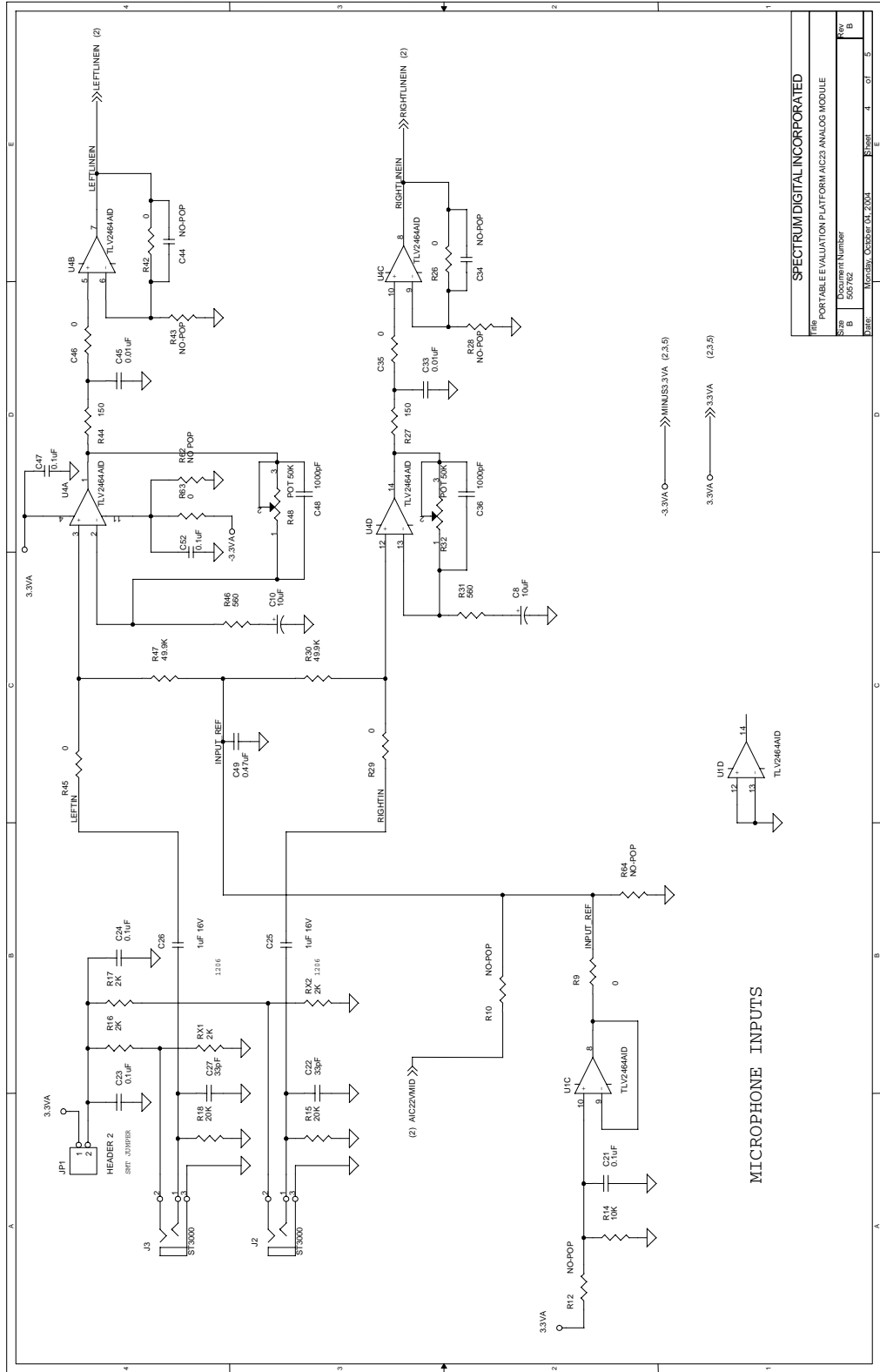


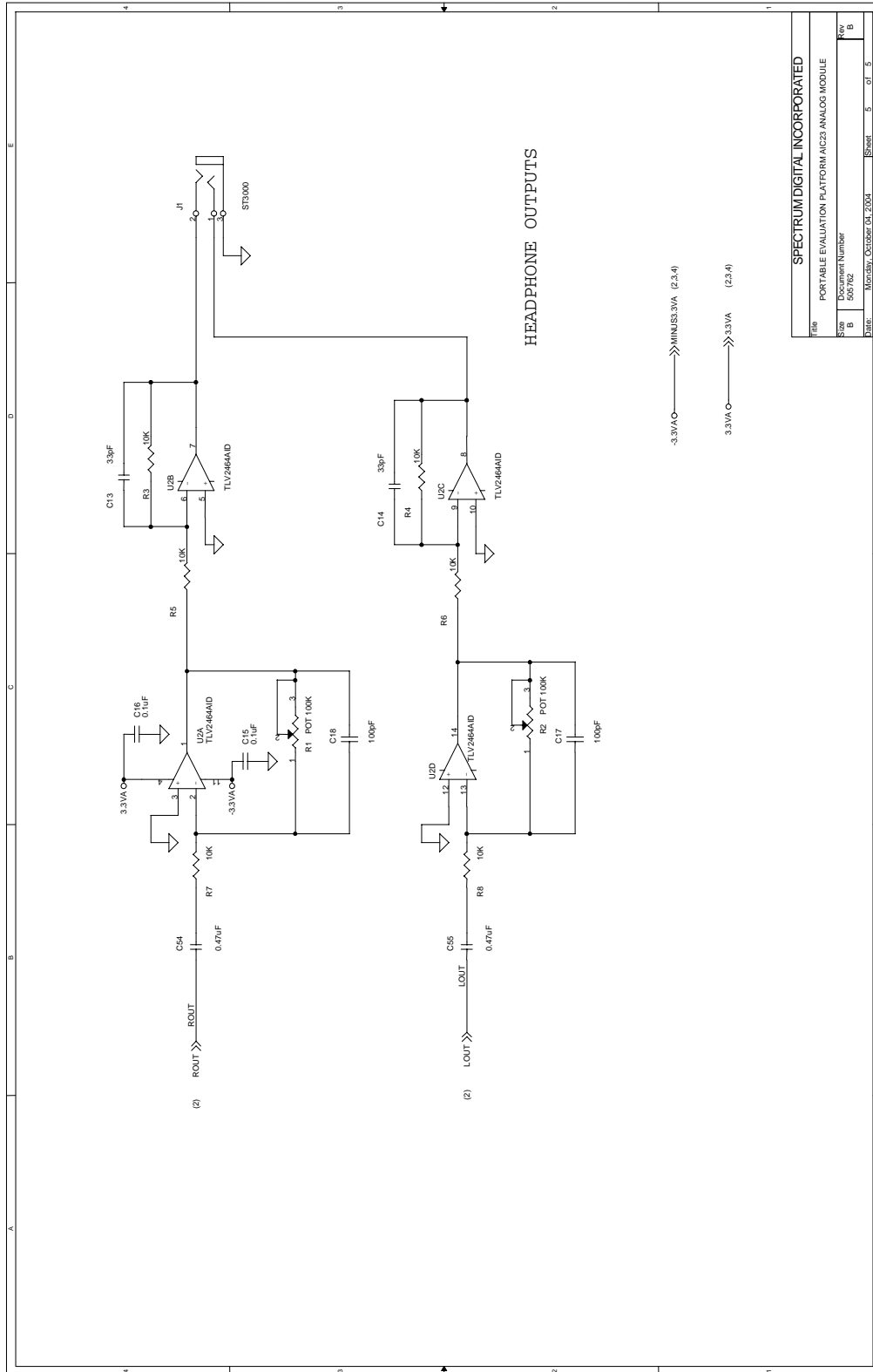
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Size	PORTABLE EVALUATION PLATFORM AIIC2365 ANALOG MODULE
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Rev	B
Date	Monday, October 04, 2004
Page	2 of 5



Part	SPECTRUM DIGITAL INCORPORATED		
Doc No	PORTABLE EVALUATION PLATFORM AIC23 ANALOG MODULE		
Rev	B	505762	
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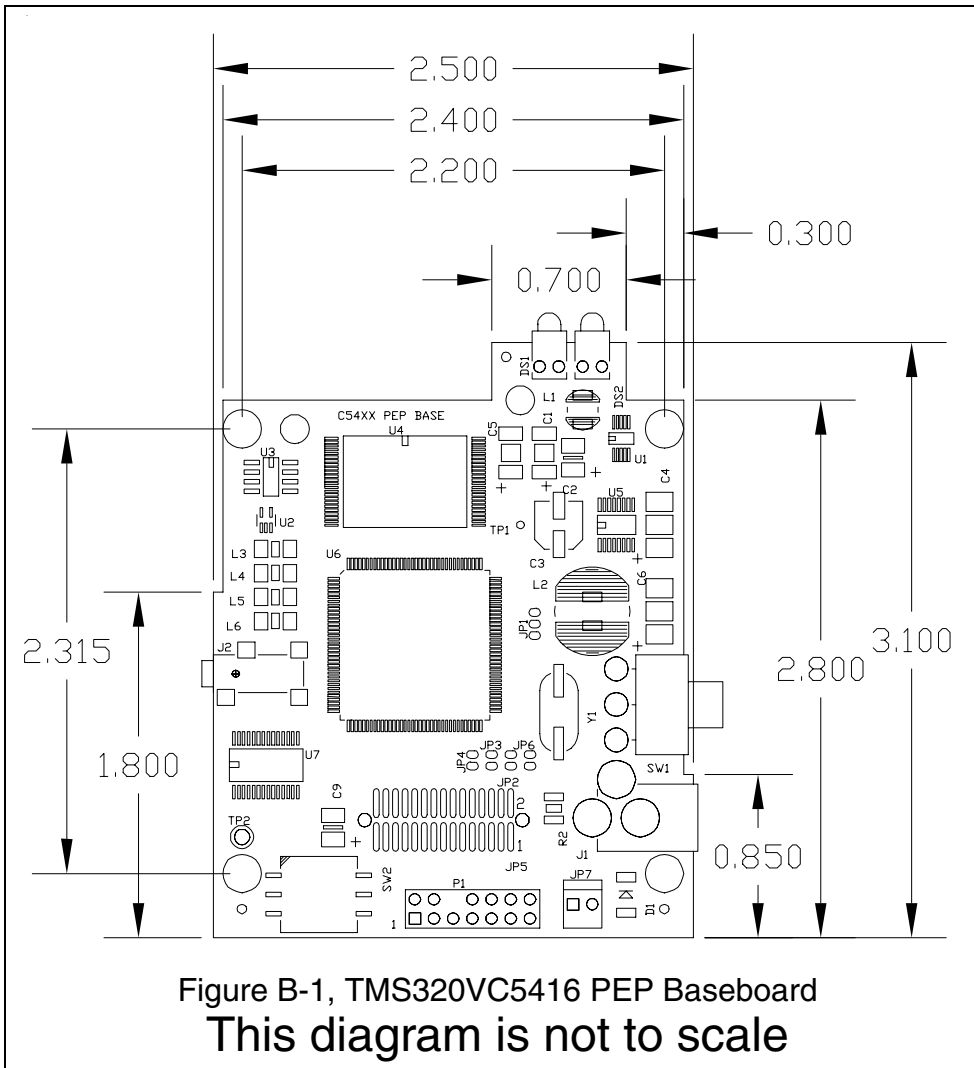
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Appendix B

TMS320VC5416 PEP Mechanical Information

This appendix contains the mechanical information about the PEP.

Topic	Page
B.1 TMS320VC5416 PEP Baseboard Mechanicals	B-2
B.2 AIC23 Daughterboard Mechanicals	B-3



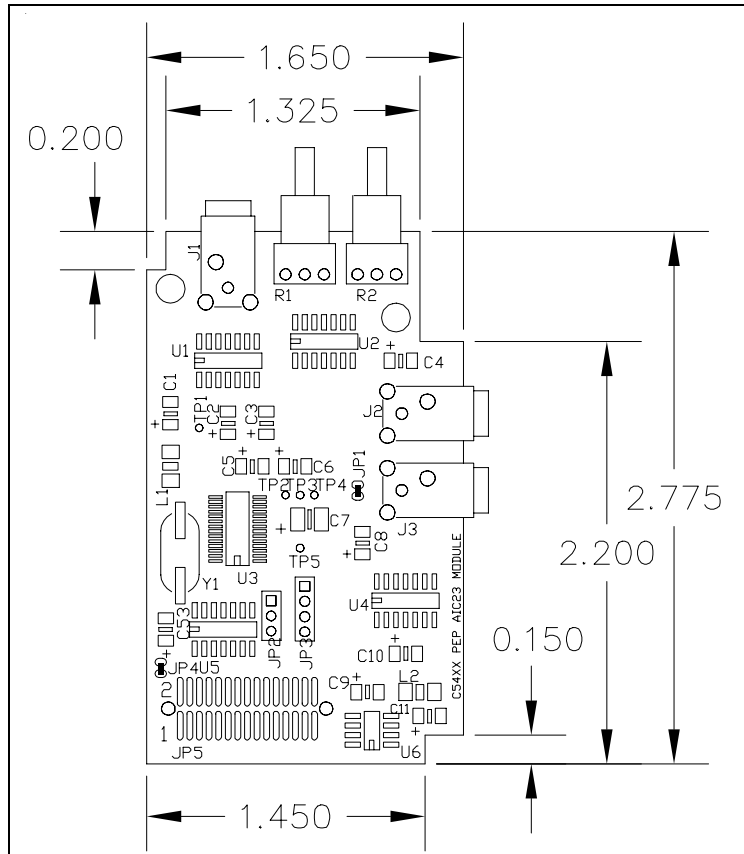
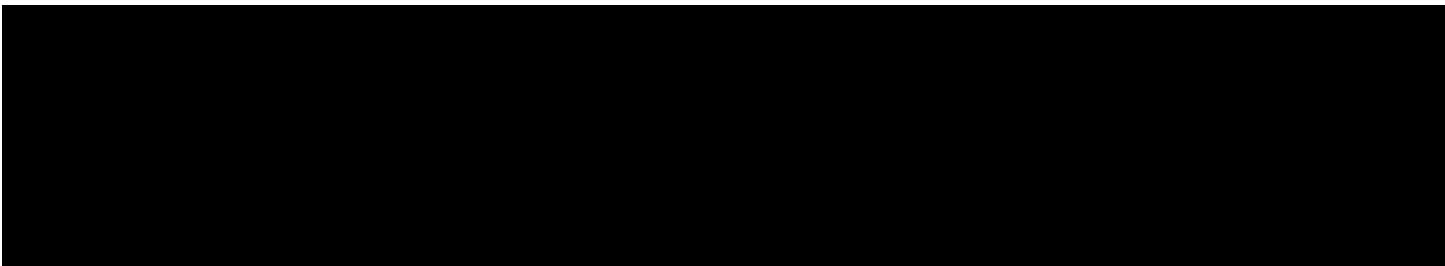


Figure B-2, AIC23 Daughterboard
This diagram is not to scale



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